SILICON EPITAXIAL LAYERS GROWN ON BURIED POROUS SILICON TEMPLATES FOR SOLAR CELLS

DETAILED ELECTRICAL AND CHEMICAL UNDERSTANDING

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Dissertation presented in partial fulfilment of the requirements for the degree of Doctor in Engineering

In collaboration with

March 2014

ISBN 978-94-6018-816-9
Wettelijk depot D/2014/7515/40

Abstract

In order to place solar power prominently in the global energy mix in the long term future, there needs to be continued cost reductions in the photovoltaic industry. In silicon photovoltaics, which forms 85-90% of the market, the cost of the silicon material itself forms a major fraction of the final solar module cost. Thus, the international technology roadmap for photovoltaic (ITRPV) forecasts a continuous reduction in the thickness of the wafer used to fabricate the solar cells.

With reduction in consumption of high quality expensive silicon as the motivation, two silicon solar cell concepts have been envisaged, namely the wafer-equivalent epitaxial silicon solar cell (WE-epicell) and the layer-transferred epitaxial silicon solar cell (LT-epicell). In both cell concepts, the entire photovoltaic power conversion occurs in a thin (20-50 μm) epitaxially-grown layer. In comparison, the thickness of a standard silicon solar cell is ~170 μm.

In WE-epicells, the epitaxial layer is grown on a low-cost and often low-purity native multi-crystalline silicon substrate, on which it remains attached in the final solar cell. In LT-epicells, the epitaxial layer is grown on a high quality mono-crystalline silicon substrate and then transferred to a low-cost carrier such as glass. The parent substrate is then re-used for the next cycle of epitaxial silicon layer transfer. In both cell concepts, porous silicon plays important functions. Porous silicon is formed by electrochemically etching a p^+ silicon substrate in an acidic electrolyte and sintering it at 1130 ^oC.

Firstly, in WE-epicells, porous silicon acts as an embedded Bragg reflector at the interface between the epitaxial layer and the low-cost substrate in order to reflect long-wavelength photons reaching the interface thereby reducing optical losses through transmission of light into the substrate, where any absorption does not contribute to the photo-generated current. In this way, the short-circuit current density of the WE-epicell is enhanced by the porous silicon Bragg reflector.

Secondly, low-cost substrates used in WE-epicells often contain significant concentration of efficiency-killing metal impurities which can diffuse into the epitaxial layer and contaminate it. In addition to its optical function, porous silicon also acts as a gettering layer to trap metal impurities at its void surfaces, effectively maintaining a relatively “clean” epitaxial layer in its proximity. This allows higher efficiency WE-epicells to be made on low-cost, low-purity silicon substrates.

Thirdly, in LT-epicells, porous silicon is the enabling technology for the layer transfer process, whereby the porosity of the porous silicon is tuned such that an elongated empty space forms within the substrate where the porous silicon is etched. This acts as the detachment layer for the layer transfer of the epitaxial layer that is grown on top.

Finally, in both cell concepts, the epitaxial layer is grown on top of annealed and sintered porous silicon. Although this is the case by design rather than choice, porous silicon also functions as a template for the epitaxial growth of high quality silicon.

The work of this thesis focuses on the in-depth study of two of these functions: (1) porous silicon as a gettering layer in the context of WE-epicells and (2) porous silicon as a template for epitaxial growth in the context of both WE-epicells and LT-epicells. Based on the theoretical and experimental understanding from these studies, suggestions for improvement of porous silicon as a gettering layer and as a template for epitaxy are proposed and implemented.

Samenvatting

Silicium epitaxiale lagen gegroeid op begraven poreus silicium structuren voor zonnecellen: diepgaande studie van de elektrische en chemische effecten

Om zonne-energie een prominente plaats in de wereldwijde energiebevoorrading te verzekeren, moet er een continue kostverlaging in de zonnecellenindustrie plaats vinden. In de silicium zonneceltechnologie, die momenteel ongeveer 85-90% marktaandeel uitmaakt in de zonnecelindustrie, is de kost van het silicium materiaal zelf verantwoordelijk voor een groot deel van de totale module kost. Daarom voorspelt de internationale roadmap voor zonne-energie (IRTPV) een continue reductie in de dikte van de silicum wafers gebruikt om de zonnecellen te produceren.

Met als motivatie een vermindering in de hoeveelheid gebruikt silicium van hoge kwaliteit, worden in deze thesis twee zonnecelconcepten bekeken, namelijk de wafer-equivalent epitaxiale zonnecel (WE-epicel) en de laag-getransfereerde epitaxiale zonnecel (LT-epicel). In beide celconcepten vindt de volledige omzetting van licht in elektriciteit plaats in een dunne (20-50 μm) epitaxiaal gegroeide laag. Ter vergelijking is de typische dikte van een standaard silicium zonnecel ongeveer 170 μm.

In WE-epicellen wordt de epitaxiale laag gegroeid op een substraat met lage kost (dikwijls een multikristallijn substraat van lage zuiverheid) en blijft de laag verbonden met dit substraat. In LT-epicellen wordt de epitaxiale laag gegroeid op een monokristallijn substraat van hoge kwaliteit en wordt deze laag nadien getransfereerd naar een goedkoop substraat zoals glas. Het moedersubstraat wordt dan opnieuw gebruikt voor een volgende cyclus van epitaxiale groei en transfer. In beide celconcepten speelt poreus silicium een belangrijke rol. Poreus silicium wordt gevormd door electrochemische etsing van een p^+ silicium substraat, waarna sintering op 1130 ^oC gebeurd.

Allereerst speelt poreus silicium in WE-epicellen de rol van Bragg reflector, die zich bevindt tussen de epitaxiale laag en het moedersubstraat om fotonen met hoge golflengtes te reflecteren en zo de optische verliezen te beperken die plaats vinden omdat licht in the moedersubstraat terecht komt waar absorptie van dit licht niet bijdraagt tot de foto-gegenereerde stroom. Op deze manier wordt de gegenereerde lichtstroom van WE-epicellen verhoogd door de poreuze silicium Bragg reflector.

Lage-kost substraten gebruikt voor WE-epicellen bevatten vaak belangrijke hoeveelheden efficiëntie - verminderende metaalonzuiver-heden die kunnen diffunderen in de epitaxiale laag en deze contamineren. Daarom speelt het poreus silicium, naast een optische rol, ook de rol van “gettering” laag die metaalonzuiverheden kan “vangen” aan de holtes in het poreus silicium. Op die manier wordt een relatief zuivere epitaxiale laag bekomen. Dit laat toe om WE epicellen van hogere efficiëntie te maken op onzuivere goedkope silicium substraten.

Daarnaast is het het poreus silicium dat in LT-epicellen toelaat om de epitaxiale laag te transfereren, waarbij het poreus silicium zodanig aangepast wordt dat een grote horizontale holte vormt in het substraat na sintering van het poreus silicium. Deze horizontale holte laat toe de epitaxiale laag die op het poreus silicium gegroeid wordt te verwijderen van het moedersubstraat.

In beide celconcepten wordt de epitaxiale laag gegroeid op poreus silicium na sintering. Poreus silicium dient daarom ook als zaadlaag voor de groei van silicium met hoge kwaliteit.

Het werk in deze thesis spitst zich toe op de diepgaande studie van 2 functies van poreus silicium: (1) poreus silicium as “gettering” laag in de context van WE-epicellen en (2) poreus silicium als zaadlaag voor epitaxiale groei in de context van zowel WE-epicellen als LT-epicellen. Gebaseerd op de theoretische en experimentale resultaten van deze thesis worden suggesties voor de verbetering van het poreus silicium als “gettering” laag en als zaadlaag voor expitaxie gemaakt en geïmplementeerd.

Dedicated to my beloved parents who ingrained in me the virtues of diligence and to Pillayar

வெள்ளத் தனைய மலர்நீட்டம் மாந்தர்தம்
உள்ளத் தனையது உயர்வு
~திருவள்ளுவர், 30 B.C.

(pronunciation)
Vella thanaya malarneetam maandhartham
Ulla thanayadhu Uyarvu

(meaning)
The height to which a lotus raises depends on the water's level
The greatness to which a man raises depends on the level of the perseverance and passion within
~Thiruvalluvar, a tamil poet, 30 B.C.

Preface

This doctoral thesis is a mosaic. At the turn of every page, there are little pieces of many selfless people who have laid little pebbles that made the path to this dissertation possible and I look back with immense gratitude.

First of all, I want to share a little anecdote. About 5 months back, I was working on my last gettering experiment. On paper it looked easy, and the idea straight-forward, but practically it was a mountain to climb, particularly because in a well-controlled environment like the IMEC clean room, "strange" experiments were given a narrow berth and wide scrutiny. So, after asking, requesting, imploring, pleading and begging my way to using various tools for each step and "steeplechasing" through Murphy's law, I was there at the penultimate step and somebody dropped another bomb. Murphy struck again!

That particular morning, somebody suddenly decided that the spinner I use for spin coating metal elements can no longer be used for that purpose because it will be used for clean "hot" lots from the P-line. This was the only reasonably-clean spinner available for my controlled experiments. It was *deja vu*. Despite my best efforts, I could do nothing to convince the persons in-charge. Totally out-of-the-blue, a by-stander, who happened to be a hardware guy, listened intently and quietly proceeded to not only find a spinner for me, but also a clean chuck. He even programmed the spinner for me. "*Go on, finish your Ph.D.*" he said with a smile. It was almost prophetic. At that moment, I had this heady feeling of incredible gratitude. I didn't care if my experiment worked. I just experienced a moment of humanity. Two days later, I bumped into him outside the clean room. I told him that I finished that final experiment. He didn't even remember who I was. Amazing. He just wanted to help. His name is Geert Doumen. I bet he doesn't remember me.

This journey of 4 years and a bit has been interspersed with moments such as these and makes the numerous trials and tribulations worthwhile in the end.

I remember at the end of my Ph.D. interview with Jef Poortmans, he concluded "*You will be a good Ph.D. student*". That was his way of accepting my candidature. I have liked his style ever since. Both my promoters, Jef Poortmans and Robert Mertens, have given me complete freedom and independence in shaping the topics and details of my thesis. After the first year, the monthly meetings with them were a morale booster for me because of their genuine interest in all my work, irrespective of whether this fits directly into the long-term strategy of the group or not. They were interested in educating me in becoming a better researcher and I am incredibly grateful for this support and guidance throughout my Ph.D. years. For all the great things they have achieved, the influence and fame they have garnered in their fields, it was refreshing to witness their great humility and impartial warmth towards everyone, no matter their status.

Fréderic Dross, who was my daily advisor for only about 4 months and the team leader of the TESS team before that, probably had the most profound influence in me and is the main reason why I finished my thesis. At two distinct periods during my Ph.D., I was so certain about quitting. I was aloof and unhappy, as if no one else had a real interest in my work except Jef and Robert. In those

doldrums of frustration, disillusionment and self-doubt, I asked Fréderic what it takes to be a good researcher and to finish a doctorate. He said the one main quality that is needed was perseverance. Not intelligence, but perseverance. It was probably the best advice I received during this thesis.

Our weekly scientific meetings were fantastic: critical and insightful. Hot knife on butter. His enthusiastic catechismal analysis of our hypotheses was so contagious that I have "templated" his scientific approach and style of communication into my work as much as possible. I realised that there is almost no limit to how deep you can go in a topic and to how broadly you can think about it. Personally, Fréderic had an "arms-around-your-shoulder" type supervisory style and pushed and motivated me to constantly expand my limits. Even after he left IMEC, he has continued to be interested in my progress. The amount of time he spent on correcting my thesis, discussing my defense slides and knuckling down to the nitty-gritty details of my thesis well beyond midnights and during weekends stands testimony to his genuine interest in my progress. I could probably write an entire chapter if I were to thank him for all his good will towards my development.

During my second year, I spent 6 weeks at Newcastle University in Prof. Nick Cowern's group for some atomistic modelling. During this time, I worked with Chihak who taught me how to do DFT simulations. Working in tandem with him was a great experience and I learnt from him the knack of simplifying a big problem into little tidbits, which I also replicated in my experimental work later on. Nick has a meticulous mind and by observing his interpretational skills, I learnt the importance of dwelling on the details and not jumping to conclusions which may be biased by our pre-conceived ideas. I still recall how he took the trouble to call me on my mobile phone while I was away on holiday in Norway to discuss about my abstract which was due the next day. He cared and that's brilliant.

Ferenc Korsós from Semilab, Hungary is the person I have collaborated with the most without actually meeting him for almost 2 full years. Finally, to break the streak, I went all the way to EUPVSEC 2013 at Paris just to meet him. He has been absolutely crucial for my thesis with his help in μ-PCD measurements. We collaborated on the basis of the best legal framework that exists: good will. It's joy to discuss things with him and I have great respect for him. He is an extraordinary person with a contagious free-mindedness, who comes up with brilliant innovations when trapped on a long-distance flights! If not for his help, I wouldn't have achieved the large number of results and in-depth understanding during the course of this thesis and so I am extremely grateful to him, Miklos and Semilab.

Ivan has been a very supportive, fair and appreciative manager. He brings great organisation and focus within the team, making all of us pull in the same direction, which made it a much better environment to work in. I realised that as a person, he is actually quite funny, warm and amicable. He showed genuine interest in my work and continued to push me to finish my thesis as soon as I can and was always there when I needed him. He wrote the Dutch version of the abstract for me on short notice on a weekend. I am grateful all he has done for me. Though my acquaintance with Jozef's was recent, each interaction with him has been pleasant and encouraging. I thank him for making our work place conducive for research.

I thank the entire i^2-module team and the larger PV group, many of whom I worked closely with and learnt a lot of things from. Valérie and Roberto are such

bright minds and it was so much fun brainstorming about the various issues surrounding porous silicon. We whipped up quite some absurd ideas and interesting experiments, but most of all, it was great fun working, chatting and joking with them. I also thank Kris who was important when it came to epitaxy-related matters and for starting up epifoils and allowing the opportunity for me to work on improving it. Twan was the master of many trades. His expertise in ultra-clean processing, gettering, passivation as well as solar cell processing came in handy throughout my Ph.D. and I always admired the fact that he has sound reasoning behind everything he says. Each word had its weight. Jonathan taught me the tips and tricks of silicone-based bonding which was crucial for lifetime measurements of epitaxial foils. He was a great team-mate to work with. Although I never personally worked with Stefano, Christos and Ounsi, they were a fantastic bunch of people with great energy, enthusiasm and good will.

Maarten Debucquoy has been immense and always made himself available for a good scientific discussion which has benefited my understanding of lifetime characterisation over the years. Maria is not just a wonderful colleague but a true friend. At the beginning of my Ph.D., when things weren't going great, she stood by me, enthused and propped me up. I often think how nice it would be if all people that I work with had the same good will and kindness towards each other. I also thank her for sorting out my epitaxy problems during Kris' absence. To me, Aude was the president of container B and I thank her for making it happy place to work. I thank Izabella for not only advising me on scientific stuff but also for sporting a happy smile every time we see each other in the cubicle. Jan Van Hoeymissen was my first supervisor and while he was at IMEC, he was very supportive of me and always defended my interests. I learnt from him that I shouldn't try to "re-invent the wheel" and when possible benefit from the expertise within IMEC. We shared a passion for photography and had some good chats when we met after he left IMEC.

I would like to also thank Niels and Sukhvinder for choosing logic and reasoning over paranoia when it came to allowing metal contaminated samples into UPSYS. I am thankful to Michael for helping with wet bench-related matters and for being so funny and sharing some nice conversations at the wet bench. At times, Loic was the go-to man when it came to questions about anything and everything that is solar cells. I thank him for patiently answering my questions. It was a pleasure working and discussing epifoils-based lifetime measurements with Savita during her thesis, when we worked like crazy past midnights and during weekends, which we might not have been motivated to do as much without the company. I would also like to thank Sathish, Prem and Marwa for helping with the XRD measurements. I am also grateful to Chantal and Pauline for their secretarial help and patience throughout these years. Karin and Greet at the IMEC library have been invaluable for their tireless supply of literature throughout the years. I thank Giovanni, Andre, Didier and Reinoud for their support, technical interventions and help at crucial times to keep tool down-times minimal. I thank many of the unknown P-line operators who have helped in processing my lots.

Eddy Simoen was an inspiring influence and his brain is like an encyclopedia. His photographic memory has always amazed me. He always made time to give important inputs throughout my thesis and I am very thankful for that. In a similar vein, I thank Paul Mertens for his insightful guidance during the sporadic meetings I organised to discuss my research problems with him. The colleagues from ultra-

clean processing (UCP) group were immense when I was setting up the procedures and process flow for my metal gettering experiments. I was able to benefit from the wealth of experience and knowledge of Jens, Kurt and Johan. Particularly, I am very grateful to Jens for the TXRF measurements and discussions. I am also thankful to Sophia, Sofie, Johnny, Kim and Adrian.

Joris and Bastien from the MCA group were absolutely fantastic in helping with SIMS measurements and often at short notice. I am also thankful to the scientists at EAG Labs for GDMS, SIMS and micro-Raman spectroscopy measurements. I would like to thank Geoffrey Pourtois for the amazing person that he is and for literally giving me personal coaching on DFT simulations before my Newcastle stay. At the beginning of my Ph.D., when I was struggling with Sentaurus simulations, Koen was always there late into the evenings and even weekends to weed out the errors in my code and explain things patiently to me and I thank him for this good will and knowledge-sharing. I thank the following collaborators: Philip Rosenits and Stefan Reber of ISE and Matthieu of Total (who was *totally* funny and amicable).

I sincerely thank the jury members: Prof. Paul Van Houtte (the chairman of the committee), Prof. Johan Driesen (the secretary for the preliminary defense), Prof. Marc Seefeldt, Prof. Nick Cowern, Sarah Kajari-Schröder and Fréderic Dross for taking part in the preliminary defense and bringing up several important aspects of the thesis for discussion which has allowed me to improve the doctoral thesis.

The better half of my Ph.D. life is the time I spent with my friends who are like my family in Europe. I thank all of them from the bottom of my heart for withstanding the test of time in the face of my idiosyncrasies, stupidities and fits of anger, happiness and craze which contrast my subdued demeanour at work.

My parents have had to face the brunt of my frustrations. I talk to them almost every day and they have been patiently listening to all my little problems and whining, joys and happiness, in equal measure.

Finally, I thank God (a co-author in all my endeavours) for bestowing upon me this opportunity, for guiding me through the trials and tribulations, and for giving me abundance of happiness and friendships to rejoice in.

Three alternative statements I would like to defend:

1. The number of pages, N, in the thesis as a function of time can be described by the following equation in analogy to the diode equation:
$$N = N_0 \exp\left(\frac{t}{t_{PD}}\right)$$
where t_{PD} is the date on which the private defense date was finalised.
2. The more you measure something, the more it improves by hook or crook. This holds true for minority carrier lifetime of an epitaxial foil as much as body weight.
3. The anti-thesis of Murphy's law: Anything that can go wrong will go wrong *transiently*, but will go right *eventually*.

Hariharsudan Sivaramakrishnan Radhakrishnan

Leuven, March 2014

Abbreviations

ALD	Atomic layer deposition
APCVD	Atmospheric pressure chemical vapour deposition
APM	Ammonium hydroxide- hydrogen peroxide mixture
BGN	Band gap narrowing
BSF	Back surface field
CCD	Charge-couple device
CG	Crystal growth
CVD	Chemical vapour deposition
Cz	Czochralski
DB	Dangling bond
DFT	Density functional theory
DIC	Differential interference contrast
DS	Directional solidification
DUV	Deep ultra-violet
EFG	Edge-defined film-fed growth
EG	Electronic grade
EL	Electroluminescence
epi	Epitaxial layer or epitaxy
feed	Feedstock
FGA	Forming gas anneal
FZ	Float zone
GD-MS	Glow discharge mass spectroscopy
GGA	Generalised gradient approximation
HP-DL	High porosity detachment layer
HR-XRD	High resolution X-ray diffraction
ICP-MS	Inductively-coupled plasma mass spectroscopy
LLI	Low-level injection
LP-TL	Low porosity template layer
LR	Learning rate
LT-	Layer-transferred
μW-PS	Microwave phase shift
μ-PCD	Microwave-detected photoconductance decay
MG	Metallurgical grade
PECVD	Plasma-enhanced chemical vapour deposition
PL	Photoluminescence

PLD	Photoluminescence decay
pre	precipitate
PS	Porous silicon
PV	Photovoltaic(s)
QSSPC	Quasi-steady state photoconductance
QSSPL	Quasi-steady state photoluminescence
ref	reference
RGS	Ribbon growth on substrate
RMS	Root-mean-squared
RTP	Rapid thermal processing
S-sites	Substitutional sites
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectroscopy
spec	specification
sim-PL	Simulation-assisted photoluminescence
SR	String ribbon
SRH	Shockley-Read-Hall
SSP	Silicon sheet from powder
sub	Substrate
T-sites	Tetrahedral interstitial sites
TCS	Trichlorosilane
tot	Total
TMAH	Tetramethyl ammonium hydroxide
TXRF	Total reflection X-ray fluorescence
UMG	Upgraded metallurgical grade
V29, V35	Void structures with a 29-atom and 35-atom sized voids
VASP	Vienna *ab initio* simulation package
WE-	Wafer-equivalent
XRD	X-ray diffraction

Symbols

Symbol	Description	Unit
Arabic		
B_{100}	Biaxial modulus corresponding to (100) plane	N m^{-2}
B_{rad}	Coefficient of radiative recombination	cm^3 s^{-1}
c_n, c_p	Electron and hole capture coefficients, respectively	cm^3 s^{-1}
C	Pre-factor or constants	-
C_v	Vacancy concentration	cm^{-3}
$C_{v,0}, C_{v,L}$	Equilibrium lattice vacancy concentration, actual lattice vacancy concentration, respectively	cm^{-3}
$C_{v,void}$	Vacancy concentration at the rim of a void	cm^{-3}
Co_{area}	Area-related costs of a PV system	€ or $
Co_{epi}	Cost of epitaxy	€ or $
Co_{other}	Area-unrelated costs of a PV system	€ or $
Co_{tot}	Total production cost per watt-peak of a PV system	€ or $
d	Thickness	µm
d_{epi}, d_{sub}	Epitaxial layer and substrate thicknesses, respectively	µm
d_{Si}, d_{PS}	Lattice parameter of silicon and porous silicon, respectively	Å
D	Diffusion coefficient	cm^2 s^{-1}
D_0	Pre-exponential factor in the diffusivity equation	cm^2 s^{-1}
D_{epi}, D_{sub}	Diffusion coefficient of minority carriers in the epitaxial layer and substrate, respectively	cm^2 s^{-1}
D_n, D_p	Diffusion coefficient of electrons and holes, respectively	cm^2 s^{-1}
D_M	Diffusion coefficient or diffusivity of metal M	cm^2 s^{-1}
E	Young's modulus	N m^{-2}
$E[\rho]$	Total energy functional of the electron density	eV
E_B	Binding energy of metal atom at a void trap site	eV
E_C, E_V	Conduction and valence band edges, respectively	eV
E_G	Band gap between conduction and valence band edges	eV
E_t	Trap/defect energy level	eV
E_T	Total energy of a system calculated using DFT	eV
f_{abs}	Absorption fraction	-
f_s	Solidification fraction of the ingot	-
G	Generation rate	cm^{-3} s^{-1}
G_{av}	Average generate rate	cm^{-3} s^{-1}
$\hat{H}$	Hamiltonian operator	-
I_{PL}	Intensity of the photoluminescence	cm^{-2} s^{-1}
$\overline{I_{PL}^{sub}}$	Fractional contribution of the substrate to the total PL intensity	-
J_{rec}	Recombination current density	mA cm^{-2}
k	Proportionality constant	-
k_B	Boltzmann constant ($= 8.61733 \times 10^{-5}$)	eV K^{-1}
$k_{eff,M}^{CG}$	Effective segregation coefficient for metal M in crystal growth technique, CG	-

k_M^0	Equilibrium segregation coefficient for metal M	-
k_σ	Defect symmetry factor	-
K_1, K_2	Constants used in Klaasen's BGN model	meV
L or L_{diff}	Diffusion length	µm
L_{epi}, L_{sub}	Minority carrier diffusion length in the epitaxial layer and substrate, respectively	µm
m	Mass	g or kg
$[M]$	Concentration of element M	cm^{-3}
M_i	Interstitial metal atom	-
M_T	Trapped metal atom	-
n	Refractive index or number or electron concentration	-/-/cm^{-3}
n_0, p_0	Electron and hole concentration in thermal equilibrium, respectively	cm^{-3}
n_1, p_1	Electron and hole SRH density, respectively	cm^{-3}
n_M	Average number of metal atoms per precipitate	-
N_c, N_v	Effective density of states in conduction and valence bands, respectively	cm^{-3}
N_{epi}, N_{sub}	Doping concentration in the epitaxial layer and substrate, respectively	cm^{-3}
N_{pre}	Precipitate density	cm^{-3}
N_t	Trap density	cm^{-3}
p	Hole concentration or number	cm^{-3}/-
P_R	Reflected microwave power	-
P_{Si}	Price of silicon feedstock	€ or $
q	Electronic charge ($= 1.602177 \times 10^{-19}$)	C
r	Radius	nm
r_c	Critical radius	nm
r_{pre}	Precipitate radius	nm
$\boldsymbol{r_i}$	Coordinates of the electrons	Å
$\boldsymbol{R_i}$	Coordinates of the nuclei	Å
R	Surface reflectivity	-
R_{d_1/d_2}	Ratio of PL intensities from samples of two different thicknesses	-
R_{rad}	radiative recombination rate	$cm^{-3}\ s^{-1}$
$[Si]$	Concentration of tetrahedral interstitial sites in silicon	cm^{-3}
S_0	Pre-exponential factor in the solubility equation	cm^{-3}
S_{BSF}	Effective surface recombination velocity due to leakage of carriers over the p/p$^+$ barrier	cm s^{-1}
$S_{defects}$	Effective surface recombination velocity due to interfacial defects	cm s^{-1}
$S_{fr}, S_{int}, S_{rear}$	Effective surface recombination velocity of front surface, interface and rear, respectively	cm s^{-1}
S_M	Solubility of metal M	cm^{-3}
S_{tot}	Sum of effective front surface and effective rear/interface recombination velocity	cm s^{-1}
t	Time	s
t_p	Duration of process step	s
T	Temperature	K or ^oC
$T[\rho]$	Total kinetic energy functional of the electron density	eV
$[T]$	Concentration of traps on the void surfaces	cm^{-3}

U	Net recombination rate	$cm^{-3}\ s^{-1}$
v_{th}	Thermal velocity	$cm\ s^{-1}$
V_0	Intrinsic vacancy volume	cm^3
$V_{ee}[\rho], V_{en}[\rho]$	Energy functionals relating to electron-electron and electron-nuclei interactions, respectively	eV
V_{OC}	Open-circuit voltage	V
$w(x)$	Intensity of the microwave probe signal	$cm^{-2}\ s^{-1}$
X_{void}, X_{Si}	Fractional concentration of metal atoms in voids and in silicon, respectively	-

Greek

α	Absorption coefficient	cm^{-1}
β	Surface curvature contribution to the chemical potential	eV
γ	Surface energy or surface tension coefficient	$eV\ m^{-2}$
δ	Skin depth	µm
$\Delta C_{v,L}$	Vacancy supersaturation	cm^{-3}
$\Delta E_{G,sub}$	Band gap narrowing	eV
ΔG_B	Gibbs free energy change for the transfer of a metal atom from a trap site to the interstitial site of the system	eV
ΔH	Change in enthalpy	eV
$\Delta n, \Delta p$	Excess electron and hole concentrations, respectively	cm^{-3}
Δn_{app}	Apparent average carrier density	cm^{-3}
Δn_{av}	Average excess carrier density	cm^{-3}
ΔP_R	Change in the reflected power of the microwave signal	-
$\Delta\sigma$	Change in conductivity	$S\ cm^{-1}$
ΔS	Change in entropy	$eV\ K^{-1}$
ΔS_v	Change in vibration entropy	$eV\ K^{-1}$
ϵ_z	Out-of-plane strain	-
η	Power conversion efficiency	-
η_{gett}	Gettering efficiency	-
θ	Fractional coverage of the void surface trap sites	-
θ_B	Bragg reflection angle	°
λ	Wavelength	nm
Λ	Dimensionless constant associated with critical radius	-
μ_0	Absolute permeability of vacuum	$N\ A^{-2}$
μ_n, μ_p	Electron and hole mobility	$m^2\ V^{-1}\ s^{-1}$
μ_r	Relative permeability of the sample	$N\ A^{-2}$
ν	Frequency of the microwave signal or Poisson's ratio	MHz/-
ρ	Resistivity	Ω cm
σ	Stress	Pa
σ_0	Dark conductivity or residual stress	$S\ m^{-1}$/Pa
σ_n, σ_p	Electron and hole carrier capture cross-sections, respectively	cm^2
σ_r	Average in-plane biaxial stress	$N\ m^{-2}$
τ	Lifetime	s
τ_{bulk}	Bulk lifetime	s
τ_{diss}	Effective lifetime after FeB pair dissociation	s

τ_{eff}	Effective lifetime	s
τ_{epi}, τ_{sub}	Bulk lifetime of epitaxial layer and substrate, respectively	s
τ_{n0}, τ_{p0}	Electron and hole capture time constants, respectively	s
τ_{pair}	Characteristic time for re-pairing of FeB pairs	min
τ_{pre}	Carrier recombination lifetime due to metal precipitate	s
τ_{rad}	Radiative recombination lifetime	s
τ_s	Surface lifetime	s
τ_{spec}	Epitaxial layer bulk lifetime specification	µs
τ_{SRH}	Shockley-Read-Hall carrier recombination lifetime	s
$\tau_{SRH,LLI}$	Shockley-Read-Hall carrier recombination lifetime under low-level injection	s
τ_{undiss}	Effective lifetime before FeB pair dissociation	s
ϕ_0	Incident flux density	$cm^{-2}\ s^{-1}$
ϕ_{ph}	Photon flux entering the epilayer	$cm^{-2}\ s^{-1}$
ψ_{bi}	Built-in potential	V
Ψ_0	Ground-state wavefunction	-
ω	Wave number	cm^{-1}
Ω	Molecular volume of silicon	cm^3

Contents

Chapter 1
Introduction

1.1 Age of the fossil fuels

"A society grows great when old men plant trees whose shade they know they shall never sit in."
~Greek proverb

There are great many number of scientists, researchers, politicians, campaigners, policy-makers, governments and non-governmental organisations and agencies who have been and are still involved in effecting a transformation in the way we produce energy for our day-to-day needs, such as transportation and power generation for residential, commercial and industrial uses.

The virtues of clean renewable energy sources as an alternative for energy produced from fossil fuels have been discussed from school text books to parliaments, *ad infinitum*. The continued growth of the world population and the increased urbanisation around the world, particularly in developing nations has resulted in a constantly growing global demand for energy, which in turn has led to the increased use of our main energy resource, fossil fuels (oil, coal and natural gas), to meet this demand [1].

"The Stone Age didn't end for lack of stone, and the oil age will end long before the world runs out of oil." ~ Sheik Ahmed Zaki Yamani, Saudi oil minister in 1970s

Predictions regarding the economically viable exploitation of oil, coal and natural gas have been largely varied and contentious. Some pessimists have predicted the end of oil and natural gas as energy resources as early as the middle of the 21st century [2], [3]. In its 2010 World Energy Outlook, the International Energy Agency (IEA) estimated that the present oil, natural gas and coal reserves would last 46, 58 and 150 years, respectively [4]. ExxonMobil, on the other hand, in its 2014 report "The Outlook for Energy: A view to 2040" predicts that there are enough oil and natural gas reserves for 125 and 200 years respectively at current production levels [1]. The World Coal Association also guarantees that there is enough coal to last more than a century at current production levels [5].

As the UK Energy Research Centre (UKERC) and International Energy Agency (IEA) pointed out (in its 2008 World Energy Outlook), it is not so much the totality of the fossil fuel reserves but rather the rate of production that is the cause for concern, particularly as the world largest oil fields start to decline [6], [7].

However, the bigger problem is the inexorable damage being done to the environment. The detrimental environmental issues such as pollution, ocean acidification, greenhouse gas emissions and resulting anthropogenic climate changes such as global warming have been much publicised in recent years [6], [8]. The negative repercussions of our unsustainable growth powered by non-renewable energy sources is no longer a remote possibility but a present reality. There is an ever-increasing clamour for the development of alternative energy technologies, as environmental issues and climate change start to have a bigger stake in policy-making decisions. A transition to a more sustainable energy source is probably the biggest challenge facing us in the 21st century.

1.2 Renewable and sustainable energy future

It has been recognised that burning out the fossil fuels to near depletion is an untenable and implausible scenario. Not only is securing our energy future important, but it is equally crucial that it is environmentally sustainable. Some have predicted that the time scale for the appearance of a new technology to replace crude oil is about 130 years from now [9]. There have been research and development into many alternative technologies such as hydroelectric power, nuclear power, wind power and solar power, to name a few.

There are obvious safety concerns associated with nuclear power, especially in the light of events such as the Fukushima disaster in 2011. Then, there is the age-old problem of disposing radioactive nuclear waste. As such, there is considerable skepticism about continued use and expansion of nuclear energy and some countries have started decommissioning their nuclear power plants [10].

In 2009, Jacobson and Delucchi presented an ambitious plan in the Scientific American journal to power the planet entirely by renewable energy sources: 51% wind power, 40% solar power and the rest from hydroelectric, geothermal and tidal power [11]. Abbreviated as WWS (wind, water and solar power), these alternative energy production technologies have already been quite successfully deployed and have potential for further expansion. Various technological, logistical, material and political constraints must be overcome before such an ambitious plan can come to fruition. It is likely that in the long-term all of these technologies will be important and will contribute to the energy mix of the future.

Of these renewable energy sources, solar power has several intrinsic advantages. As illustrated in Figure 1. 1 (a), solar energy is by far the largest source of inexhaustible power available to us [12] and according to the Intergovernmental Panel on Climate Change (IPCC), has the highest global technical potential of all renewable energy sources [13]. It is widely deployable and not constrained by the source. It has the highest energy density by land surface area compared to all other renewable energy sources [12].

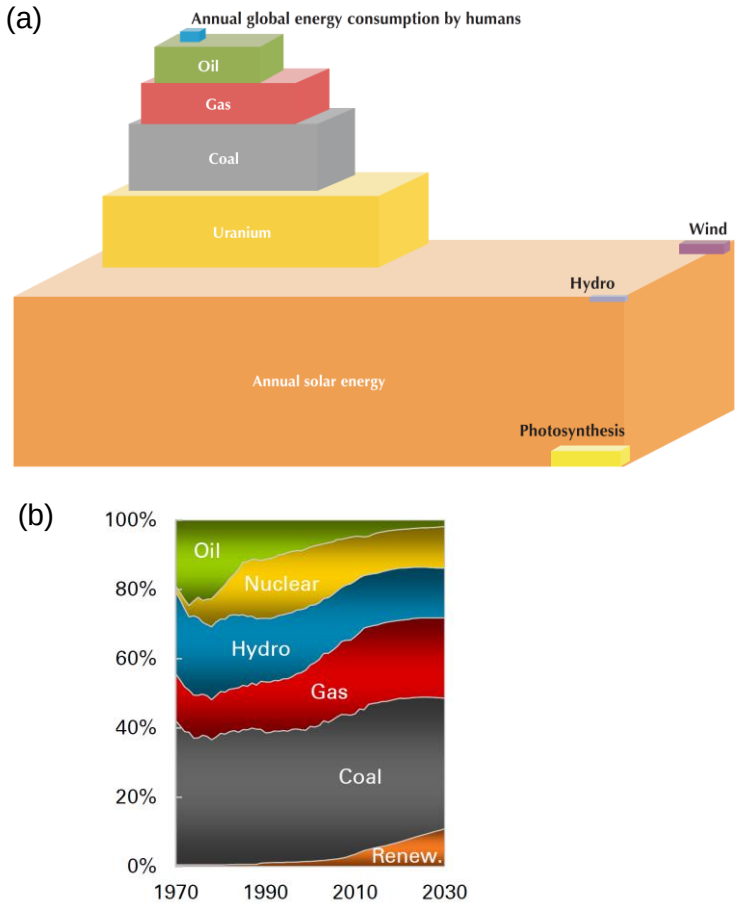

Figure 1. 1 (a) Total energy resources available to us (from [12]*). (b) Historical and forecasted contributions from different energy sectors towards power generation (from* [14]*).*

Given its immense potential, the photovoltaic (PV) market has been experiencing extraordinary growth over the past decade with an annual growth rate of ~40% [15], with Europe and in particular Germany and Italy leading the growth of the PV installations. In 2012, the milestone of surpassing the 100 GW cumulative installed global PV capacity was surpassed [10]. However, as noted by the European Photovoltaic Industry Association (EPIA), the PV market is starting to be truly global with countries such as China, the USA, Japan and India ramping up their solar energy programmes [10]. As such, the IEA expects the solar energy sector to be the fastest growing market in the coming decades, and has projected solar power to provide > 10% of global electricity by 2050 [4]. ExxonMobil has made similar projections towards 2040, forecasting a 60% in the renewable energy sector, leading to 10% of global electricity coming from wind and solar power alone in 2040 [1]. Similar forecasting by BP is shown in Figure 1. 1 (b) [14].

1.3 The "Moore's law" of silicon photovoltaics

Of all the different PV technologies, silicon photovoltaics dominates about 85-90% of the market [15]. This success can be attributed to the fact that it is a proven technology, benefiting from material and process research from the microelectronics industry which is largely based on silicon. Moreover, silicon is the second most abundant material on earth. Silicon modules also have long lifetimes. Added to these, the crystalline silicon PV market has gone through tremendous price reductions over the past decades. So, we can expect crystalline silicon PV to dominate in the years to come.

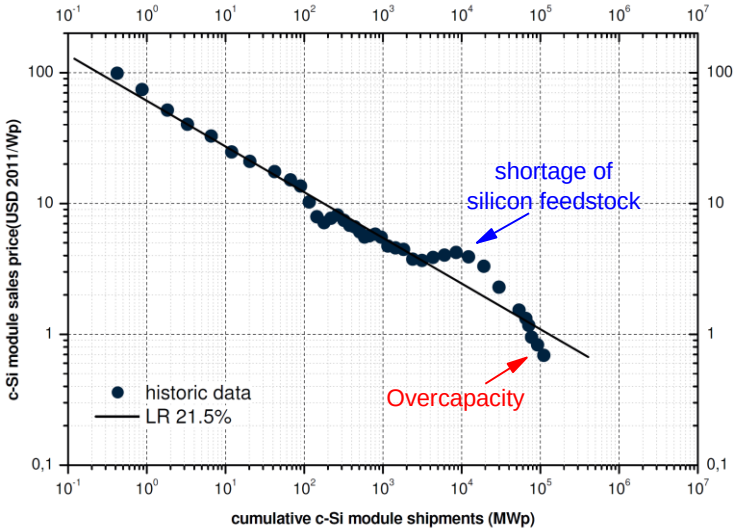

Figure 1. 2 PV learning curve: the average crystalline silicon module price as a function of the cumulative crystalline silicon module shipments (from [16], [17]*).*

Figure 1. 2 shows the learning curve of crystalline silicon photovoltaics [16], [17], which shows the average selling price of a crystalline silicon module per watt-peak (US$/$W_p$) as a function of the cumulative module shipments in megawatt-peak. A learning rate (LR) plot of 21.5% is superimposed on the historical data, which implies that for every doubling of the cumulative shipments, there is about 21.5% reduction in the price of the modules. This learning rate is the highest in the energy world. The learning rates of 1% for hydro-electric power, 5% for geothermal power and 7-9% for wind power fade in comparison [12]. Two major aberrations can be noticed and they can be attributed to a shortage of silicon feedstock around 2004-2007 and an overcapacity around 2012-2013 [12], [17]. Despite these, the PV market is set to continue at its average historical LR in future.

The major factors that interplay to result in the cost reductions observed in Figure 1. 2, are module power conversion efficiency, manufacturing plant size, silicon feedstock cost and process complexity. Increase in efficiency, up-scaling of the plant size, reduction in silicon cost and processing simplicity all contribute to the large learning rate of crystalline silicon PV [18], [19]. The total cost of silicon (which is the sum of useful silicon used in cell processing and the silicon lost in the kerf during wire sawing) forms a major fraction of the final module cost. In 2010,

the cost of silicon formed 42% of the module cost while in 2013, this was still 29%. Thus, a reduction in the usage of silicon will contribute strongly to cost reductions. The International Technology Roadmap for Photovoltaics (ITRPV) predicts a continued reduction in the silicon wafer thickness as shown in Figure 1. 3.

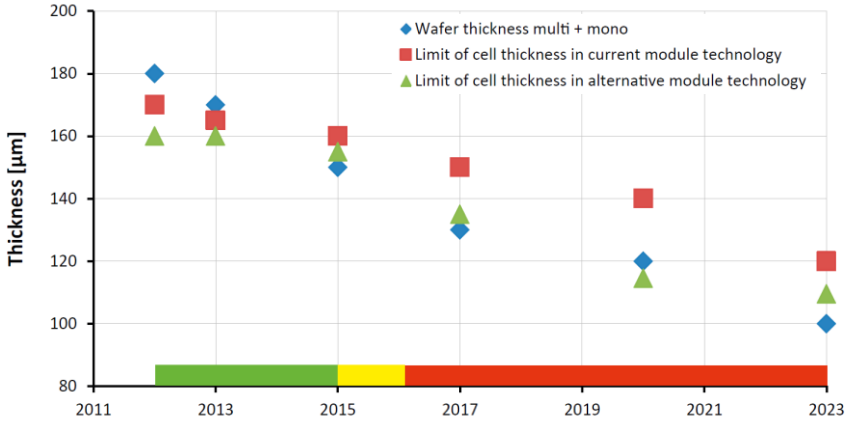

Figure 1. 3 Predicted trend for minimum as-cut wafer thickness in mass production of solar cells and minimum cell thickness in module manufacturing (from [17]*). The green bar along the horizontal axis indicates the presence of an industrial solution for processing cells with the indicated thicknesses in the corresponding module technology. The red bar indicates the absence of such a solution while the yellow bar indicates that an industrial solution exists but is not yet in mass production.*

1.4 Thin film crystalline silicon solar cells grown by epitaxy

State-of-the-art monocrystalline silicon solar cell with a conversion efficiency of 25.0% in a small area cell of 4.00 cm^2 and the highest crystalline silicon module efficiency of 22.9% have been achieved using complex processes and high quality expensive silicon [20]. Meanwhile, in the thin film silicon world, amorphous silicon / microcrystalline silicon solar modules which have the advantages of low silicon consumption, low-cost processes and direct module integration result in the highest module efficiencies of ~10% for single-junction devices [21]. This illustrates the trade-off explained in the preceding section. On the one hand, very high efficiencies are made possible by increased process complexity and silicon cost. On the other hand, low-cost process and lower silicon cost meant a low efficiency module. An optimum must be found.

In this section, two cell concepts are presented which aim to combine the higher efficiency advantage of bulk crystalline silicon solar cells and lower cost advantage of thin film silicon solar cells. In both cell types, the entire active layer where photovoltaic power conversion occurs is grown epitaxially.

1.4.1 Wafer-equivalent epitaxial silicon solar cell (WE-epicell)

A detailed review of wafer-equivalent epitaxial silicon solar cells (WE-epicells) grown on native silicon substrates is given by Poortmans and Arkhipov in [22] as well as McCann *et al.* in [23]. The institutes and companies active in this field are Fraunhofer Institute for Solar Energy Systems (ISE) [24], Scifiniti [25] and IMEC [26], [27].

A WE-epicell consists of a high-quality active layer of ~20-30 µm thickness, grown epitaxially on top of a 150-200 µm thick, low-cost and typically low-purity p^+ silicon substrate. Since the substrate is heavily-doped and is of low quality, active photovoltaic power conversion is effectively confined to the thin high quality epitaxial layer. The substrate, therefore, merely acts as a conductive, mechanical support and provides a crystal template for the epitaxial growth of the active layer.

The p^+ silicon substrate used in a WE-epicell is usually of low-quality and low-purity that is obtained from inexpensive crystal growth techniques (such as directional casting or string ribbon techniques) and using cheap feedstock (such as metallurgical grade silicon or upgraded metallurgical grade silicon). Thus, the amount of high quality and therefore expensive silicon that is used in WE-epicells is minimal (20-30 µm) compared to a standard high quality bulk crystalline silicon solar cell (150-200 µm). In this way, the total cost of silicon in the WE-epicell concept is lowered in comparison to standard crystalline silicon solar cells, making it an economically attractive proposition [26], provided the energy conversion efficiency is high enough to advocate the merits of this cell concept. Porous silicon, which is indicated in Figure 1. 4 as voids in silicon, plays a critical role in improving the efficiency potential of this cell concept, as will be outlined in the next section.

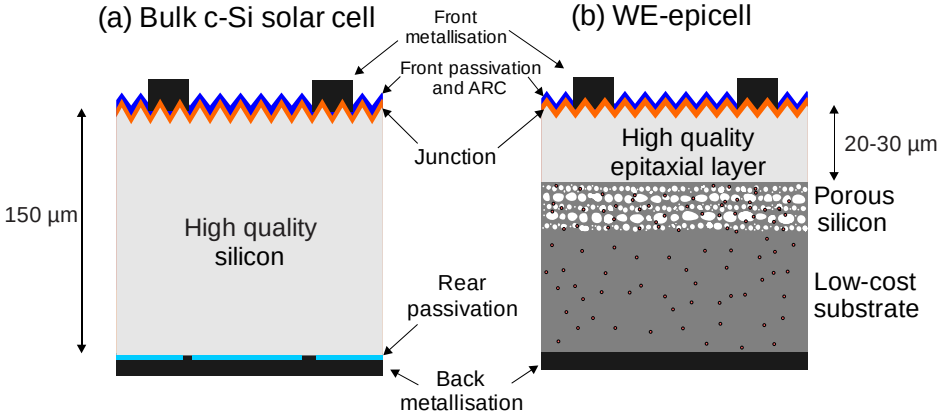

Figure 1. 4 Cross-sectional schematics of (a) a two-side contacted, bulk crystalline silicon solar cell, and (b) an epitaxial wafer-equivalent silicon solar cell (WE-epicell). The black dots in the low-cost substrate indicate metal impurities.

A typical WE-epicell (as it is fabricated at IMEC) is shown next to a standard bulk silicon solar cell in Figure 1. 4, indicating the numerous similarities between the two cell types. Besides porous silicon etching and silicon epitaxy, all other processes are similar in both cell types. Thus, the barriers for adoption of the WE-

epicell into existing wafer-based production lines is minimal. This is why this epitaxial cell concept is called "wafer-equivalent".

The WE-epicell also has several disadvantages. Firstly, since low-cost feedstock is used, the substrate would contain significant concentrations of detrimental metal impurities. If these impurities diffuse into the epitaxial layer during high temperature process steps, the cell efficiency would be severely reduced.

Secondly, since low-cost crystallisation methods are used for the growth of the substrate, the defect density in the substrate could be very high depending on the method. This would affect the quality of the epitaxial layer grown on top, thus limiting the efficiency potential of the epitaxial layer.

Thirdly, the interface between the epitaxial layer and the substrate is not accessible for passivation. So, the "rear" of the epitaxial layer is in fact the high-low p/p^+ junction, and such an interface cannot achieve a low effective interface recombination velocity especially in the presence of an embedded porous silicon layer as shown in Figure 1. 4 (b).

Finally, the epitaxial layer is optically thin, since silicon is an indirect band gap material. This would lead to significant optical losses through transmission of infrared photons into the substrate, where any absorption would not contribute towards the photo-generated current.

1.4.2 Layer-transferred epitaxial silicon solar cell (LT-epicell)

A second approach to minimise the amount of high quality silicon used in the cell is growing a thin epitaxial layer of ~30-50 µm on a high quality p^+ monocrystalline substrate and then transferring the thin silicon layer to a cheaper carrier such as a glass superstrate which provides the mechanical support for the thin layer for further processing into solar cells. Since this cell concept involves transfer of a thin silicon layer from one carrier (p^+ silicon substrate) to another (glass superstrate), it is called layer-transferred epitaxial silicon solar cell (LT-epicell).

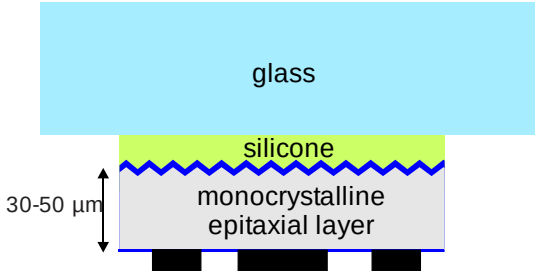

Figure 1. 5 Cross-sectional schematic of a layer-transferred epicell (LT-epicell), showing a thin monocrystalline epitaxial layer attached to a glass carrier.

The cross-section schematic of a LT-epicell is shown in Figure 1. 5, which depicts a monocrystalline epitaxial layer attached to a glass carrier using silicone. As with WE-epicells, the amount of silicon used in this concept is only ~30-50 µm which is significantly less than wafer-based silicon solar cells. Furthermore, in comparison to amorphous silicon, microcrystalline silicon or polycrystalline silicon thin film solar cells, this layer-transferred epitaxial layer is mono-crystalline (since

it is grown on a monocrystalline wafer before layer transfer) which guarantees significantly higher power conversion efficiencies for LT-epicells.

In addition, LT-epicells also have the intrinsic advantage of integrating module level processing together with cell processing if the epitaxial layer is transferred directly to glass. Thus, several tiles of epitaxial silicon can be transferred to a large sheet of glass and subsequently processed in an integrated and parallel fashion at the module level, resulting in a higher throughput. The disadvantage, however, is that binning the cells according to their power output at the end of the module processing flow is not possible. This could lead to losses due to mismatched solar cells.

As shown in Figure 1. 5, the presence of silicone restricts the processes after layer transfer to low temperature steps. Lower temperature process steps are usually less expensive and this further reduces the cost of LT-epicells. On the other hand, since this cell concept is far away from the typical processing sequence of bulk crystalline silicon solar cells, process developments dedicated to LT-epicells must be carried out which could initially lead to process complexities which might increase the cost.

Finally, LT-epicells not only use less silicon, but also have negligible kerf loss of ~4-5 µm compared to ~100 µm kerf loss for bulk wafer-based silicon solar cells. This is a significant advantage which leads to further cost reduction for LT-epicells.

1.5 Porous silicon in epitaxial solar cells

As alluded to earlier, porous silicon plays crucial roles in both types of epitaxial silicon solar cells, introduced in the preceding section. The content of this thesis revolves around these different functions of porous silicon in the two epitaxial silicon solar cells, which will be presented in this section.

1.5.1 Porous silicon formation and sintering

In the work of this thesis, porous silicon is formed by means of electrochemical etching of a heavily-doped p^+ silicon substrate in a hydrofluoric acid (HF)-based electrolyte, as shown in Figure 1. 6. The p^+ silicon substrate forms the anode of the electrochemical cell while platinum is used as the cathode. Pore formation in silicon in HF-based electrolytes is only possible in anodic conditions with a current density that is below a critical current density. Above this current density, electropolishing occurs. Details of the electrochemistry of silicon electrodes in acidic electrolytes as well as the different pore formation mechanisms can be found in [28].

The following explanations about porous silicon formation mechanisms are based on the book “Electrochemistry of Silicon” by Lehmann [28]. The divalent electrochemical dissolution of silicon during anodic etching begins with hole injection from the bulk towards the interface between silicon and the electrolyte (see step 1 of Figure 1. 7). This initiates a nucleophilic attack of the surface silicon atom by either HF molecules, $(HF)_2$ dimers or hydrogen bifluoride ions (HF_2^-). Once a Si-F bond forms, a second nucleophilic attack is initiated with an accompanying electron injection into the substrate (step 2 in Figure 1. 7), but this

step does not require a hole injection. The highly electronegative F atom in the Si-F bond makes it easier for the a Si atom bonded to two F atoms to be easily attacked by other molecules and dissolution quickly proceeds (steps 3-5 in Figure 1. 7). The dissolved silicon remains in solution as SiF_6^- molecule. Thus, the reaction can be written as

$$Si + 4HF_2^- + h^+ \rightarrow SiF_6^- + H_2 + e^- \quad (1.1)$$

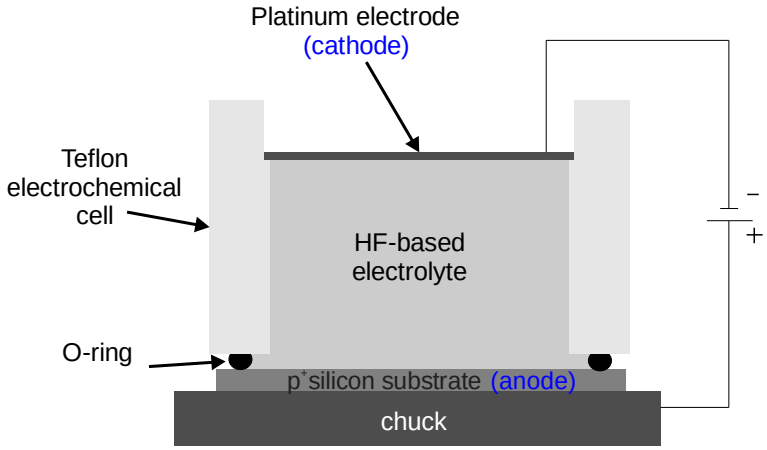

Figure 1. 6 Schematic diagram of the porous silicon etching set-up used in the work of this thesis. Anodic etching of p⁺ silicon in HF-based electrolytes are performed in a telflon cell that is resistant to HF.

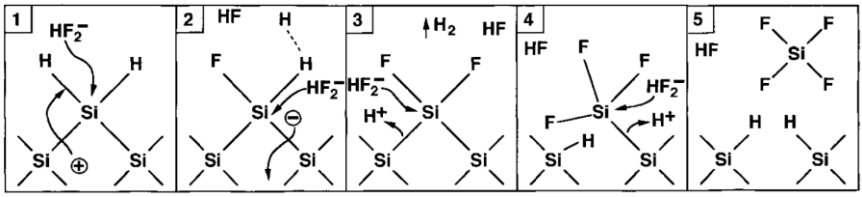

Figure 1. 7 Reaction mechanism for the divalent dissolution of silicon in anodic conditions in a HF-based electrolyte (from [28]*).*

In the above reaction mechanism, hole injection is the rate-limiting step and is the key to the formation of pores. When a p-type silicon electrode is connected in anodic conditions in a HF-based electrolyte, the depletion region exists on the surface of the silicon anode and charge carrier transport is by band-to-band tunneling through the space charge region. When a current is applied, pits nucleate on the surface and grow approximately perpendicular into the surface. As the etching proceeds, dissolution of silicon only proceeds at the pore tips rather than the pore walls. This is because for silicon dissolution, holes are needed. Since a depletion region forms in p-type silicon in acidic electrolytes, the pore walls are passivated by the depletion of holes. Since holes are only available at the pore tips, where due to the curvature of the pore tip, there is also a strong electric field, pore growth proceeds at the pore tips.

The resulting morphology is a dendritic mesh of mostly columnar pores with diameters of ~10-50 nm, depending on the current density applied. Increasing the current density of the etching process increases the etch rate as well as the porosity. By fixing the current density and varying the etch time, precise porous silicon thicknesses can be obtained. The porosity and etch rates of the porous silicon can also be varied by electrolyte concentration or silicon doping concentration but these were kept constant in the work of this thesis.

In both WE-epicells and LT-epicells, epitaxy is carried out on top of porous silicon. However, a pitted surface with the channels of the pore opening to the surface is not amenable for high quality epitaxial growth and will leads to a large defect density in the epitaxial layer. Thus, after porous silicon etching, the sample is annealed at a high temperature of 1130 ^{o}C in a hydrogen ambient at atmospheric pressure for a typical time of 10 min, to smoothen out the surface. During the annealing process, the porous silicon sinters, whereby the ~10-50 nm thick columnar pores coalesce to form large spheroidal voids in silicon in the range of ~40-200 nm, depending on the porosity and thickness of the porous silicon layer. The driving force for this sintering process is the minimisation of total energy (especially surface energy) by means of vacancy diffusion [29], [30]. Intrinsic stress might also play a role in which case the minimisation of the total energy also includes the strain energy [31]. This is dealt with in further detail in Chapter 7. This reorganisation step is important because it results in a quasi-monocrystalline surface which is better suited for epitaxial growth than an as-etched surface.

Despite being a better template, annealed porous silicon is still far from the ideal template for epitaxial growth. However, since both cell concepts rely on the growth of epitaxial films on annealed porous silicon, the quality of these epitaxial layers must be assessed and the potential for high quality layers to be grown on annealed porous silicon templates must be studied. This forms a major part of the work of this thesis.

1.5.2 Roles of porous silicon in WE-epicells

As explained earlier, WE-epicells can suffer from efficiency reduction due to optical transmission losses of long-wavelength photons and due to contamination of the epitaxial layer from metal impurities diffusing from the low-quality substrate. These issues are addressed by using a porous silicon layer.

In order to reduce transmission losses in WE-epicells, long wavelength photons (with small absorption coefficient) reaching the interface of the epitaxial layer with the substrate must be reflected at the interface. In this way, their optical path length in the epitaxial layer can be enhanced, giving these photons a greater chance to be absorbed in the epitaxial layer and thus contribute to the photo-generated current. Such a reflector can be for instance a silicon dioxide interlayer reflector [24] or a porous silicon Bragg reflector as is the case for WE-epicells fabricated at IMEC [32].

A Bragg reflector consists of a stack of alternating layers of two different refractive indices, n_L and n_H. The two different refractive indices are implemented in porous silicon by using two different porosities (low and high porosities, referred by the abbreviations, L and H). The physical thickness of each layer, d_i, is determined by the quarter-wavelength rule for constructive interference

$$d_i = \frac{\lambda}{4n_i} \tag{1.2}$$

where λ is the wavelength of peak reflectance for the Bragg reflector and i is either L or H, corresponding to each layer type (low or high porosity).

The refractive index of porous silicon lies in between those of air and silicon, and can be described by various effective medium theories, depending on the morphology (as-etched versus annealed) of the porous silicon. Increasing the porosity of the porous silicon results in a decrease of the refractive index. Thus, by modulating the current density with time, a depth modulation of the porosity of the porous silicon and thus refractive index is attained. The as-etched and annealed Bragg reflector displaying the alternating porosity structure is shown in Figure 1. 8.

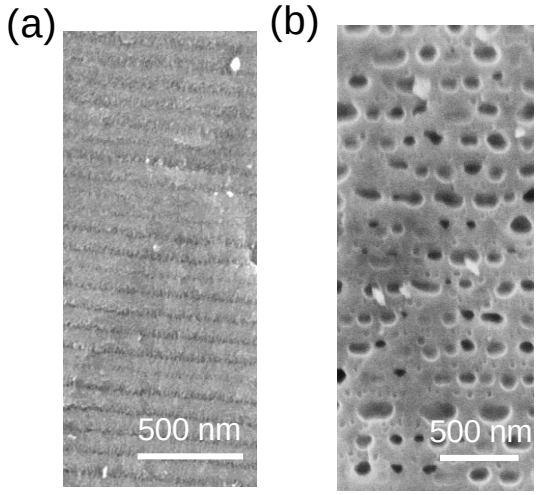

Figure 1. 8 Scanning electron microscopy image of an (a) as-etched, and (b) annealed porous silicon-based Bragg reflector, showing alternating layers of different porosity.

The beneficial effect of porous silicon as a Bragg reflector has already been extensively studied [27], [32]–[34]. By implementing a well-optimised simple Bragg reflector, significant improvement in the internal quantum efficiency in the long wavelength range has been observed. This resulted in an increase in the short-circuit current density of ~3.1 $mAcm^{-2}$ and an accompanying efficiency improvement of ~1.5% [34]. By using an advanced chirped reflector, which is a superposition of many Bragg reflectors designed at different wavelengths, an increase in the bandwidth of reflection has also been achieved. This has resulted in an enhancement in the short-circuit current density of ~5.4 $mAcm^{-2}$ and an associated efficiency improvement of 2.7% [32]. Thus, it is clear the porous silicon as a Bragg reflector is crucial in the enhancing the efficiency of WE-epicells.

The second challenge with WE-epicells is the mitigation of detrimental metal impurity diffusion from the substrate into the epitaxial layer during high temperature process such as the epitaxial growth itself. It was envisaged that porous silicon can also act as a gettering layer to reduce the epitaxial layer contamination problem. Porous silicon gettering has been studied in the

purification of metallurgical grade silicon [35] while cavity gettering has been researched by various groups for microelectronics [36]–[38]. Thus far, only preliminary indications have been given that porous silicon could indeed acts as a gettering layer in epitaxial solar cells [39], [40]. This function of porous silicon as a gettering layer is studied in depth in this thesis.

Additionally, annealed porous silicon also functions as a template for the epitaxial growth of silicon. This is also studied in detail in this thesis.

1.5.3 Roles of porous silicon in LT-epicells

The essence of LT-epicells is the layer transfer of an epitaxial layer from the silicon substrate on which it is grown. Porous silicon can perform the function of a detachment layer to allow the lift-off of the epitaxial film. Several groups have been actively involved in research and development of kerf-less layer transfer techniques to produce very thin (< 50 μm) silicon. The electrochemically-etched porous silicon-based layer transfer approach is one such promising technique that was first proposed by Tayanaka et al. [41]. Porous silicon is in fact the enabling technology for this route.

An extensive review of this approach in its various embodiments (Sintered porous silicon (SPS) of Sony [41] and University of Stuttgart [42], [43], Porous silicon process (PSI) of ZAE Bayern [44], [45]) and other associated methods is given by Brendel [46]. Other groups that have also been developing the layer transfer of thin silicon during the early years include Institut National des Sciences Appliquées de Lyon (INSA Lyon) [47] and IMEC [48], [49]. Presently, several institutes and companies are active in this field such as Institute for Solar energy Research (ISFH) [50]–[52], Solexel [53], Crystal Solar [54], Episun [55], AmberWave [56] and IMEC [57].

Integral to the layer transfer process is a double layer stack of porous silicon (a low porosity template layer (LP-TL) of ~1-2 μm on top of a high porosity detachment layer (HP-DL) of ~300 nm) that is electrochemically-etched on a highly-doped silicon substrate (step 1 in Figure 1. 10). Similar to the WE-epicells, after etching, the porous silicon is sintered at a high temperature and the as-etched, fine columnar pores reorganize such that the HP-DL becomes a large extended void interrupted by tiny pillars while the LP-TL transforms into smaller spheroidal voids embedded in a monocrystalline silicon matrix such that the surface is ideally free of open voids (step 2 in Figure 1. 10). The scanning electron microscopy images of as-etched and reorganised porous silicon stacks are shown in Figure 1. 9.

On the annealed porous silicon surface, a monocrystalline epitaxial silicon layer of ~30-50 μm thickness can be grown (step 3 in Figure 1. 10). These epitaxial layers can be easily detached from the silicon parent substrates using a mechanically weak HP-DL. However, the handling of thin silicon films (which can be called epitaxial foils or epifoils when free-standing) after detachment from the parent substrate in a free-standing configuration will lead to increased yield loss due to breakages. In order to overcome this issue, the epitaxial film can first be front-side (sunny side) processed while attached to the parent substrate (step 4 in Figure 1. 10) and then bonded to a superstrate glass using silicone as glue.

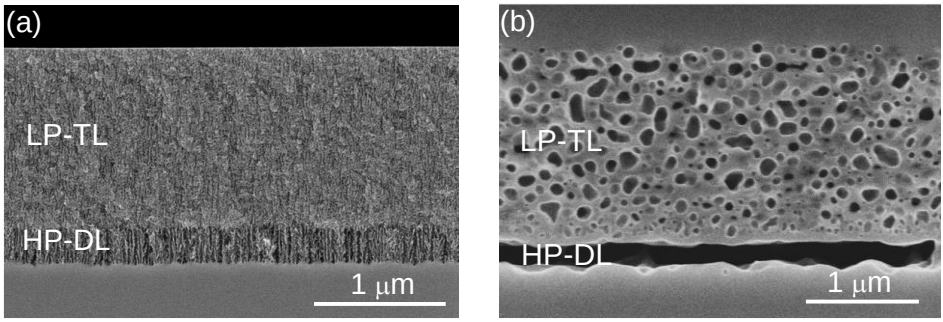

Figure 1. 9 Scanning electron microscopy image of an (a) as-etched, and (b) annealed porous silicon stack used in the layer transfer process. Note that an epitaxial layer has been grown on top of the annealed porous silicon in (b). LP-TL refers to the low porosity template layer and HP-DL refers to the high porosity detachment layer.

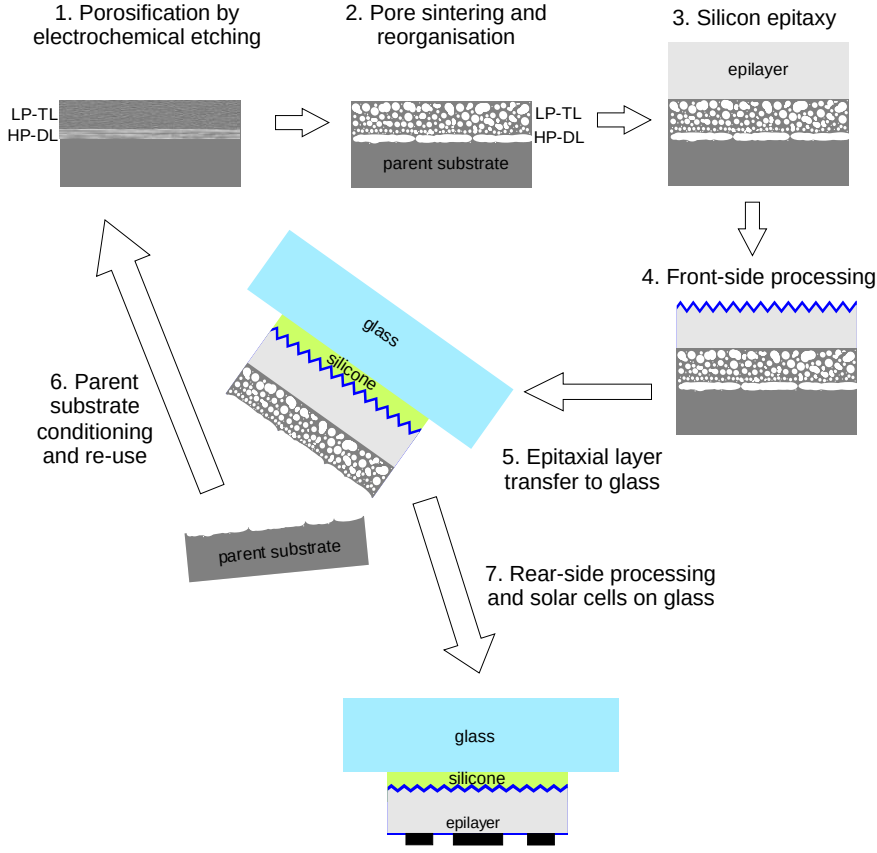

Figure 1. 10 The process flow for the fabrication of a layer-transferred epitaxial silicon solar cell, showing the details of the porous silicon-based layer transfer process.

Subsequently, the epitaxial film can be detached from the parent substrate, resulting in the layer transfer of the film to the glass superstrate (step 5 in Figure 1.

10). The detached epifoil, now bonded to glass, can be further processed into solar cells (step 7 in Figure 1. 10) and the parent substrate can be conditioned for reuse in the next cycle of layer transfer of an epitaxial film (step 6 in Figure 1. 10). In this way, the thin foils are never handled free-standing. Several groups including IMEC follow this route [55], [58]. Alternatively, the epitaxial film can be rear-side (dark side) processed while it is still attached to the parent substrate and then layer-transferred to a conductive substrate before the front-side is processed while bonded to the foreign substrate. This is the approach followed by AmberWave, where the epitaxial film is transferred to a steel substrate [56].

Although cell processing after the silicon foil is bonded to glass has its constraints and complications (since compatibility with glass and silicone is essential), conversion efficiencies of ~18% have been achieved on solar cells processed with FZ silicon bonded to glass prior to rear-side processing [58]. More impressively, Solexel has announced its world record conversion efficiency of > 20% on 156 mm by 156 mm full-square solar cells using a 43 μm-thick epitaxial silicon in a back-contact / back-junction configuration [12].

As mentioned before, besides enabling the layer transfer process itself, annealed porous silicon (LP-TL) obviously also acts as the template for the epitaxial growth of silicon. Since the efficiency potential of this concept is very much dependent on the bulk lifetime of the epitaxial layer, the role of porous silicon as a template becomes rather important, particularly in this cell concept.

1.6 Thesis outline

In this thesis, the functions of porous silicon as a gettering layer and as a template for epitaxial growth are studied in depth.

Chapters 2, 3 and 4 deal with porous silicon as a gettering layer. Chapter 2 starts by motivating quantitatively the necessity for gettering in WE-epicells. Subsequently, theoretical modeling work is done to understand the strength of metal gettering at the void surfaces of porous silicon. In particular, first principle calculations based on density functional theory are used for calculating metal binding to void surfaces. In addition, diffusion modeling is performed to estimate the gettering efficiency of porous silicon.

In Chapter 3, the results of intentional metal contamination and gettering studies are reported. Both chemical/elemental and electrical analyses are used to estimate the gettering efficiency of porous silicon for iron, nickel and copper. The results from the different methods are compared verifying the reliability of the obtained gettering efficiencies.

In Chapter 4, the possibility of tuning the properties of porous silicon to enhance the gettering efficiency of porous silicon is explored. Both theoretical and experimental studies are combined to indicate the right approach towards enhanced gettering.

Chapters 5, 6 and 7 deal with the function of porous silicon as a template for epitaxial growth, studied mainly using lifetime measurements. Chapter 5 introduces theoretically the different lifetime measurement methodologies which

are needed to understand lifetime measurements on both attached epitaxial layers (as in WE-epicells) and detached epitaxial foils (as in LT-epicells).

In Chapter 6, experimental proof of high quality epitaxial growth on anneal porous silicon is presented. Appropriate reference structures are used for comparison. The theoretical results from Chapter 5 are used to understand the results.

In Chapter 7, the approach towards improving the epitaxial layer quality by tuning the porous silicon properties is presented. Indications are also given towards achieving high detachment yield without compromising on epitaxial layer quality for LT-epicells.

Chapter 8 concludes the main results of the thesis and provides an outlook towards future work for each topic.

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Chapter 2
Transition Metal Gettering by Porous Silicon: Theory and Modeling

This chapter discusses the theoretical aspects of porous silicon gettering, with a particular focus on WE-epicells. In the first part, the importance of porous silicon gettering in the context of WE-epicells is explained. This is done by introducing the potential low-cost feedstock and crystallisation techniques available for fabricating low-cost substrates. Subsequently, the detrimental effects of transition metals in silicon is explained. Based on these, a methodology for deriving a metal contamination specification level for low-cost substrates and low-cost feedstock for use in WE-epicells is presented. In the second part, the potential of porous silicon as a gettering layer to mitigate the detrimental effects of metal impurities in WE-epicells is discussed. *Ab initio* calculations using density functional theory and diffusion modelling are used to understand metal binding to void surfaces.

2.1 Importance of metal gettering in WE-epicells

In wafer-equivalent epitaxial silicon solar cells ("WE-epicells"), the active region of the solar cell is effectively confined to the 20-30 μm thick electronic- or solar-grade epitaxial layer that is grown on top of the heavily-doped p^+ silicon substrate. The purity requirements for the substrate material itself is relaxed to lower the cost of WE-epicells. This opens up the possibility of employing a wide range of relatively inexpensive crystalline silicon substrates.

2.1.1 Possible candidates for low-cost silicon substrates

The work of this thesis only concerns WE-epicells grown on native crystalline silicon substrates, rather than foreign substrates such as ceramics or glass. There are several advantages in using low-cost silicon substrates over low-cost foreign substrates. Firstly, the thermal expansion coefficient of a silicon substrate is obviously well-matched with the growing epitaxial layer. Secondly, besides

providing mechanical support for the thin epitaxial layer, the chief role of the silicon substrate is to act as a template for the epitaxial growth of silicon. Since the crystal structure of the native silicon substrate is copied during epitaxy, this allows epitaxial layers with a large grain size to be grown. For example, if multi-crystalline low-cost silicon substrates are used, grain sizes in the order of a few centimetres can be obtained. On the contrary, silicon deposition on foreign substrates using various techniques typically yields grain sizes in the range 1-10 μm [1]–[4], although up to 100 μm have been reported [5].

In the production of wafers for the electronics industry, silica is used as the raw material in an arc furnace to produce metallurgical grade (MG) silicon that is 99% pure. Silicon purity is expressed either in percentage or in terms of the number of nines in the purity percentage specification, N. So, MG silicon has 2N purity and contains a high concentration of a variety of impurities such as iron, copper, nickel, titanium, vanadium, aluminium, boron and phosphorus among others [6], [7]. Silicon with such high levels of impurities is neither useful for electronics fabrication nor solar cell fabrication. Thus, MG silicon is first reacted with hydrochloric acid to form chlorosilanes. These chlorosilanes are distilled to purify the silane precursors which are then used in the Siemens chemical vapour deposition (CVD) process to produce ultra-pure polycrystalline silicon rods. These rods are used as feedstock in mono-crystalline crystal growth techniques such as the Czochralski (Cz) process for producing electronic grade (EG) silicon ingots with a 8-9N purity. The distillation of chlorosilanes and the Siemens CVD process are both energy-intensive and energy-inefficient processes, requiring > 120 kWh/kg of EG polycrystalline silicon feedstock [7].

For WE-epicells, where the substrate is inactive for the purposes of photovoltaic power generation, such high purity levels or such expensive growth techniques are unnecessary and not viable. The cost of silicon substrates used for WE-epicells can be reduced in two ways: (1) by using cheap silicon feedstock, and/or (2) by using low-cost crystalline silicon growth techniques.

Low-cost feedstock options

One of the cheapest silicon sources is MG silicon, which only costs US$1.5-2/kg [8] and uses about 14-16 kWh/kg of energy [7]. MG silicon can also be refined and purified using various energy-efficient techniques to produce upgraded metallurgical grade (UMG) silicon, which has ~4-5N purity. These techniques include acid leaching, melting with vacuum treatment, plasma reaction and/or treatment with reactive gases, as well as optimised directional solidification described in detail in [9], [10]. Of these, directional solidification is an attractive option because it is not a dedicated purification step but essentially a crystal growth technique which leads to multi-crystalline silicon ingots.

During directional solidification, molten silicon in a crucible is solidified from the bottom to the top, resulting in long columnar grains with a diameter in the order of centimeters [11]. The additional benefit of this technique is that most of impurities (especially metal impurities) have a higher solubility in the liquid phase and therefore segregate to the melt as the solidification front moves to the top of the ingot [12]–[15]. As a result, only the top of the ingot is heavily-contaminated,

while most of the ingot is purified through this segregation process, described by the Scheil equation [12] as

$$[M]_s = [M]_{feed} k_{eff,M}^{DS} (1 - f_s)^{k_{eff,M}^{DS} - 1} \quad (2.1)$$

where $[M]_s$ is the concentration of impurity M in the solidified ingot, $[M]_{feed}$ is the concentration of the impurity M in the feedstock, $k_{eff,M}^{DS} > k_M^0$ is the effective segregation coefficient (which is the non-equilibrium ratio of concentration of impurity M in the solid over that in the liquid) of impurity M for the directional solidification (DS) process and k_M^0 is the equilibrium segregation coefficient. f_s is the solidification fraction. The $k_{eff,M}^{DS}$ values for different impurities are given in Table 2. 1. From this, it is clear that purification by a factor of above 10^3 can be obtained for the transition metal impurities, while boron and phosphorus cannot be effectively removed. However, this is not an issue since for WE-epicells, highly-doped wafers are required as noted in Chapter 1.

Table 2. 1 Segregation coefficient of different impurities during the directional solidification process (from reference [14]*)*

Impurity	Effective segregation coefficient for directional solidification process, $k_{eff,M}^{DS}$
B	~1
P	~1
Fe	1.6×10^{-4}
Ni	9.0×10^{-4}
Cu	2.0×10^{-3}
Cr	3.7×10^{-3}
Ti	2.5×10^{-3}

Table 2. 2 Impurity concentrations found in electronic grade (EG) silicon, metallurgical grade (MG) silicon and upgraded metallurgical grade (UMG) silicon. Data have been compiled from various references.

Impurity	EG [ppb] [6]	MG [ppm] [6], [16]	UMG [ppm] [14]	UMG [ppm] [16]	UMG [ppm] [7]
Al		1000-4350	2	0.16	0.15
B	<0.1	40-60	2.2	3.3	2
Fe	0.1-1.0	1550-6500	<1	0.13	<0.05
Ni	0.1-0.5	10-105		0.031	<0.01
Cu	0.1	15-45		0.046	<0.01
Cr	<0.01	50-200		0.009	<0.005
Ti		140-300	<1		<0.005

In Table 2. 2, the typical concentrations of impurities found in MG silicon, EG silicon as well as UMG silicon is given as a compilation of data from literature. Thus,

using MG or UMG silicon as the feedstock can lower the cost of production of wafers for WE-epicells.

Furthermore, EG silicon wafers having high doping levels that are out of the specification limits, are rejected by the electronics industry. This highly-doped "rejected/off-spec" silicon is also a viable candidate for use as substrates for epitaxial cells by virtue of the fact that it is highly-conducting and exceeds the required purity levels. In addition, waste silicon wafers from electronics industry may be reclaimed by removing the fabricated circuitry in the top layer. Therefore, besides MG and UMG silicon feedstock, the "rejected/off-spec" and "reclaimed" silicon can also be considered as alternative sources of "cheap" silicon feedstock for WE-epicells [17].

Low-cost crystal growth techniques

There are two main categories of low-cost crystal growth techniques: silicon casting and silicon ribbon growth.

Multi-crystalline ingots grown by silicon casting methods (silicon casting or directional solidification) are wire-sawn into thin multi-crystalline wafers that can be used as substrates for WE-epicells. This results in grains in the order of centimetres and dislocation densities of $< 10^5$ cm^{-2}. While the cost of these cast multi-crystalline wafers is lower than single-crystal growth techniques, due to their lower purification costs, a significant amount of the cast silicon is still lost while slicing the grown ingot into bricks and during wire-sawing of the wafers.

On the other hand, a second set of crystal growth techniques, collectively called silicon ribbon techniques, that produce wafers directly from the melt eliminates these kerf losses by rendering the wire-sawing process unnecessary. If the same quality as cast multi-crystalline wafers can be maintained, this should lead to lower-cost silicon substrates. Among more than a dozen silicon ribbon techniques, the most successful and representative methods have been reviewed in detail by Hahn and Schoenecker [18], McCann et al. [19] and Kalejs [20].

Silicon ribbon growth methods can be further sub-divided into three groups. In the first group, typified by edge-defined film-fed growth (EFG) ribbon, String Ribbon (SR) and Dendritic web growth, the ribbon is pulled vertically out of the melt such that the growth direction is the same as the pulling direction. No supporting substrate is required in these methods. For the case of Dendritic Web growth, single crystalline ribbons are produced with odd numbers of twinning planes and have a dislocations density of only $\sim 10^4$ cm^{-2} [11]. EFG and SR both produce multi-crystalline ribbon with large (1-10 mm wide) grains elongated along the growth direction, with defect densities of $\sim 10^5$-10^6 cm^{-2} [19]–[21].

In the second group, exemplified by Ribbon Growth on Substrate (RGS) and Molden Wafer (previously known as Silicon Film™), the growth front is perpendicular to the pulling direction and a substrate is needed to support the growing film. Since the growth direction and pulling directions are decoupled, these methods have much higher throughput. However, they produce multi-crystalline silicon ribbons with small grains in the range of 10-500 μm, and usually with a higher defect density of $\sim 10^5$-10^8 cm^{-2} [19], [20], compared to the first group described above.

Finally, in the third group, represented by Silicon Sheet from Powder (SSP), compacted silicon powder is heated from one side such that some of surface granules melt and percolate into the underlying powder. The resulting ribbons have grains in the order of 0.15-1.5 mm, although this can be improved to have cm-sized grains by a zone melting recrystallisation (ZMR) process [19]. The dislocation density is $\sim 10^6$-10^7 cm^{-2}. More recently, research has been ongoing on producing substrates by sintering of silicon powder by spark plasma [22] or hot pressing [23], [24] and by thermal spraying techniques [22].

Similar to directional solidification, purification of the silicon ribbons through segregation of transition metal impurities in the melt occurs also during the ribbon growth techniques. The effective segregation coefficient, $k_{eff,M}^{CG}$, for the impurity M depends strongly on the crystal growth technique, CG, and the growth conditions (see Table 2. 3). For instance, for RGS and Silicon Film™ ribbons, since the growth interface is perpendicular to pull direction, impurity segregation into the melt is not efficient.

Table 2. 3 The effective segregation coefficient, $k_{eff,M}^{CG}$ of transition metal impurities M for the different crystal growth(CG) techniques are given based on [14], [20].

Growth method	Effective segregation coefficient for different crystal growth (CG) techniques, $k_{eff,M}^{CG}$
Direction solidification	$k_M^0 < k_{eff,M}^{CG} < 10^{-3}$
EFG	$k_M^0 < k_{eff,M}^{CG} < 10^{-3}$
SR	$k_M^0 < k_{eff,M}^{CG} < 10^{-3}$
RGS	~ 1
Silicon Film™	~ 1

WE-epicells on different low-cost substrates and feedstocks

The first WE-epicell on a low-cost substrate was fabricated as early as 1976 by Kressel *et al.* on a EFG ribbon resulting in an efficiency of ~10% [25]. Various attempts at fabricating WE-epicells on some of these substrates based on different feedstock quality using various epitaxial deposition techniques and cell processes at several different institutes are summarised in Table 2. 4. In general, it is difficult to compare epicells fabricated at different institutions with different cell processing steps and material parameters. However, from Table 2. 4, it can be seen that several institutes have shown WE-epicells fabricated on high quality p^+ Cz wafers to have conversion efficiencies of >17% and open-circuit voltages of >650 mV, demonstrating the potential of WE-epicells. Furthermore, cells fabricated on low-cost p^+ UMG/offspec/reclaimed silicon multi-crystalline wafers show lower efficiencies (~12-13%) and open-circuit voltages (590-620 mV), particularly when no gettering steps are included. Only when a porous silicon layer (which acts as both a Bragg reflector and a gettering layer) is incorporated, the efficiency improves to ~15%. Finally, for the case of cells fabricated on RGS and SSP substrates, which have a much higher dislocation density and much smaller grain sizes, the efficiencies are very low at ~8%.

Table 2. 4 Summary of WE-epicells fabricated on different substrate types using different cell process flows in different institutes, showing the efficiency, η, and open-circuit voltage, V_{OC}, obtained. Where it is known, the feedstock quality is specified. APCVD and RTCVD refer to atmospheric pressure and rapid thermal CVD, respectively. "sc" refers to "single-crystalline" and "mc" refers to "multi-crystalline".

Substrate type	Feedstock quality	Deposition method and thickness	η, V_{OC}	Remarks	Institute
p^+ sc-Si, Czochralski	EG	RTCVD, 37 µm	17.6%, 661 mV	n-p-n-p-n structure	ISE[1] [26]
	EG	CVD, 17 µm	17.6%, 664 mV		UNSW[2] [27]
	EG	APCVD, 48 µm	17.3%, 655 mV		MPI-FKF[3] [28]
	EG	APCVD, 25 µm	16.9%, 627 mV		IMEC [29]
p^+ mc-Si, Direction Solidification	UMG	RTCVD, 30 µm	13.1%, 594 mV		ISE [26]
	UMG	APCVD, 20 µm	12.8%, 607 mV	no gettering	IMEC [17]
	Off-spec	APCVD, 20 µm	12.5%, 605 mV	1 h $POCl_3$ gettering	IMEC [17]
	Off-spec	CVD, 19 µm	15.2%, 627 mV	Porous silicon reflector and gettering	IMEC/ISE [30]
	Reclaimed	APCVD, 20 µm	12.8%, 618 mV	1 h $POCl_3$ gettering	IMEC [17]
p^+ mc-Si, EFG		CVD, 47 µm	10.0%, 560 mV	AM-1 radiation	RCA[4] [25]
p^+ mc-Si, RGS		CVD, 24 µm	8.6%, 513 mV		IMEC [31]
p^+ mc-Si, SSP		RTCVD, 15 µm	8.0%, 553 mV		ISE [26]

[1]ISE stands for Fraunhofer Institute for Solar Energy Systems

[2]UNSW stands for University of New South Wales

[3]MPI-FKF stands for Max-Planck-Institut für Festkörperforschung

[4]RCA refers to RCA Laboratories, Princeton

These observations appear to indicate that the substrate influences the efficiency potential of WE-epicells in two major ways. Firstly, even though it has been observed that the crystal quality of epitaxial layers grown on low-cost substrates can be better in terms of the dislocation density since not all the dislocations of the substrate are copied during epitaxial growth [19], [25], the grain size and intra-grain dislocation density of the epitaxial layer seems to be proportional to that of the substrate. Thus, ribbon growth techniques where a supporting substrate is used during the growth process (e.g. RGS or SSP) may not

be suitable due to their high dislocation densities and small grain sizes. Silicon substrates from directional solidification and dendritic web growth (and to an extent EFG and SR) appear to be promising candidates for WE-epicells due to their lower dislocation densities.

Secondly, there would be considerable amount of metal impurities in the low-cost substrates due to the low-purity feedstock used as raw material. Even if higher quality feedstock ("off-spec") is used, the low-cost growth technique itself can incorporate considerable amount of metal impurities during the growth process [14], [32]. These metal impurities will out-diffuse into the epitaxial layer during high temperatures processes such as epitaxy and lower the quality of the epitaxial layer. Thus, an effective gettering layer is needed to mitigate the effect of the metal contaminants in the substrate on the epitaxial layer such that it remains viable for high efficiency solar cell fabrication. For this purpose, porous silicon can be used as an intermediate gettering layer to reduce epitaxial layer contamination by the substrate. The study of porous silicon gettering forms the essence of this chapter.

2.1.2 Detrimental effects of metal impurities present in low-cost substrates

Recombination activity of transition metal impurities in silicon

Transition metal impurities exist as either point defects in interstitial or substitutional lattice locations or as precipitated clusters in silicon. In either form, transition metals in silicon are detrimental to solar cell function because they act as recombination centres for minority carriers by forming deep levels in the band gap of silicon. Recombination that is facilitated by defect levels in the band gap is called Shockley-Read-Hall (SRH) recombination [33], [34]. In low to moderately-doped silicon, this is the predominant recombination channel.

The SRH minority carrier lifetime, τ_{SRH}, due to a deep level defect of bulk concentration, N_t, with an energy level, E_t, located in the band gap of silicon, having electron and hole capture cross sections of, σ_n and σ_p, respectively is given by [33], [34]

$$\tau_{SRH} = \frac{\tau_{n0}(p_0 + p_1 + \Delta n) + \tau_{p0}(n_0 + n_1 + \Delta n)}{n_0 + p_0 + \Delta n} \tag{2.2}$$

where

$$\tau_{n0} = \frac{1}{\sigma_n v_{th} N_t}, \quad \tau_{p0} = \frac{1}{\sigma_p v_{th} N_t} \tag{2.3}$$

and

$$n_1 = N_c \mathrm{e}^{\left(-\frac{E_C - E_t}{k_B T}\right)}, \quad p_1 = N_v \mathrm{e}^{\left(-\frac{E_t - E_V}{k_B T}\right)} \tag{2.4}$$

τ_{n0} and τ_{p0} are the capture time constants of electrons and holes, respectively. v_{th} is the thermal velocity taken to be $\sim 10^7$ cm/s. n_0 and p_0 are the thermal equilibrium electron and hole concentrations, respectively, while n_1 and p_1 are the equilibrium densities of electrons and holes when the Fermi level, E_F, coincides with the defect level, E_t. E_C and E_V are the conduction and valence band edges. Δn is the excess minority carrier concentration in p-type silicon. Carrier trapping is assumed to be negligible i.e. $\Delta n = \Delta p$. N_c and N_v are the effective density of states in the conduction and valence bands, respectively.

A symmetry factor, k_σ can be defined for each defect, which is the ratio of the electron to hole capture cross-sections

$$k_\sigma = \frac{\sigma_n}{\sigma_p} = \frac{\tau_{p0}}{\tau_{n0}} \tag{2.5}$$

Deep levels in the band gap can either be donor type or acceptor type. A donor type defect level is neutral when occupied by an electron and positively charged when empty. An acceptor type defect level is neutral when it is unoccupied by an electron and negatively charged when occupied. There can also be double donor or double acceptor levels. Often transition metals have more than one defect level in the band gap. In that case, usually the deeper level is assumed to be the dominant level for recombination processes [35], [36]. There has been extensive research using deep-level transient spectroscopy (DLTS), electron paramagnetic resonance (EPR), Hall effect studies, injection-dependent lifetime spectroscopy (IDLS) and temperature-dependent lifetime spectroscopy (TDLS) to identify and obtain the defect level in the band gap of silicon for various transition metal impurities as well as their associated carrier capture cross sections. There is a large variation and/or uncertainties in the reported values in literature. The dominant defect energy level in the band gap of silicon of some common transition metal impurities and their associated electron and hole capture cross-sections is given in Table 2. 5.

Table 2. 5 The dominant defect energy level in the band gap of silicon of some common transition metal impurities and their associated electron and hole capture cross-sections at room temperature are given based on various literature reports. The corresponding symmetry factor is also listed.

Impurity	E_t [eV]	σ_n [cm^2]	σ_p[cm^2]	k_σ	Reference
Ti (dd)	$E_V + 0.28$	1.5×10^{-15}	3.7×10^{-17}	40.5	[40], [41]
Cr (d)	$E_C - 0.24$	2×10^{-14}	4×10^{-15}	5.0	[38], [39]
CrB (d)	$E_V + 0.28$	2×10^{-14}	1×10^{-14}	2.0	[39]
Fe (d)	$E_V + 0.38$	7.5×10^{-15}	6.6×10^{-17}	113	[42], [43]
FeB (a)	$E_C - 0.26$	3.3×10^{-15}	1.4×10^{-15}	2.34	[43], [44]
Ni (a) in p-type Si	$E_V + 0.40$	5.6×10^{-17}	8×10^{-17}	0.70	[37]
Ni (d) in n-type Si	$E_C - 0.19$	3.9×10^{-12}	1.1×10^{-15}	3545	[37]
Cu (a)	$E_V + 0.43$	$> 3 \times 10^{-13}$	$< 8 \times 10^{-17}$		[45]
Cu (d)	$E_V + 0.23$	$> 1.4 \times 10^{-14}$	3×10^{-16}		[45]

"d" stands for donor, "dd" stands for double donor and "a" stands for acceptor

A brief summary is given here for selected $3d$ transition metals, namely titanium (Ti), chromium (Cr), iron (Fe), nickel (Ni) and copper (Cu). Titanium is an interstitial impurity and has three defect levels in the band gap: an accepter level at $E_C - 0.08$ eV, a donor level at $E_C - 0.27$ eV and a double donor level at at $E_v + 0.28$ eV, but it is believed that the double donor level is the dominant

recombination channel [37]. Titanium has large carrier capture cross-sections, particularly for electrons, as summarised in Table 2. 5.

A Cr interstitial defect has a donor type level at $E_C - 0.24$ in the band gap of silicon [38], [39]. In boron-doped silicon, Cr pairs with boron (B) to form the donor type chromium-boron (CrB) defect with a level at $E_V + 0.28$ [39]. Carrier capture cross-sections are larger than that of Ti.

Iron impurities predominantly exist as interstitial impurities with a donor type defect level at $E_V + 0.38$ eV [37], [41], [42]. Similar to Cr, in boron-doped silicon, Fe tends to be paired with B to form the iron-boron (FeB) defect. The FeB defect has two known defect levels: a donor level at $E_V + 0.1$ eV [36], [41], [46] and an acceptor level at at $E_C - 0.26$ eV [37], [44]. It is generally accepted that the deeper acceptor level is the dominant recombination channel [36]. While there is reasonably agreement about the carrier capture cross-sections for interstitial iron (Fe_i), there is a large uncertainty for the FeB defect. In Table 2. 5, the most recent values reported by the group of Macdonald (Australian National University) are given[1] [43]. Moreover, there is a large asymmetry in the carrier capture cross-sections for Fe_i compared FeB, as seen from the symmetry factor, k_σ, of 113 and 2.34 respectively [42].

Nickel predominantly exists as substitutional impurity with the dominant acceptor type defect level in p-type silicon at $E_V + 0.40$ eV and the dominant donor type defect level in n-type silicon at $E_C - 0.19$ eV [37]. Despite having a rather deep level in the silicon band gap, the capture cross-sections for the defect level active in p-type silicon are smaller than the metal impurities discussed so far.

Copper has been a difficult impurity to study due to its extremely high diffusivity and solubility in silicon. Thus, the recombination parameters for Cu point defects have not been obtained with certainty.

Defect levels that have large minority carrier capture cross sections and energy levels close to the centre of the band gap are the most detrimental recombination centres. The SRH lifetime of eqn. (2.2) can be simplified under low level injection (LLI) conditions, depending on the location of the energy level of the defect in the band gap of silicon [37], [47]. For transition metal interstitials forming deep level defects in p-type silicon, a useful simplification for LLI conditions is

$$\tau_{SRH,LLI} = \tau_{n0} = \frac{1}{\sigma_n v_{th} N_t} \tag{2.6}$$

As noted earlier, 3d transition metals (e.g. Fe, Co, Ni and Cu) can form silicon-rich silicide precipitates in silicon of the form MSi_2 except copper which forms Cu_3Si [41], [48]. Such precipitates can vary in size depending on contamination level, thermal budget and density of nucleation sites. For tiny silicide precipitates (< 5 nm), the SRH lifetime can be computed using eqns. (2.2) or (2.6). Plekhanov and Tan have also shown that the capture cross-sections of such precipitates can be very high (10^{-12}-10^{-10} cm^2) compared to the point defects (see Table 2. 5) [50]. On the other hand, for large precipitates (>50 nm) the SRH recombination lifetime

[1] Macdonald and co-workers have been active in studying the recombination parameters of interstitial iron and iron-boron pairs over more than a decade [43], [44], [46], [85]–[87].

in p-type silicon with a precipitate density, N_{pre}, and precipitate radius, r_{pre}, has been derived by Cañizo [49]

$$\tau_{pre} = \frac{1}{4\pi r_{pre} D_n N_{pre}} \tag{2.7}$$

where D_n is the diffusion coefficient of the minority carrier electron.

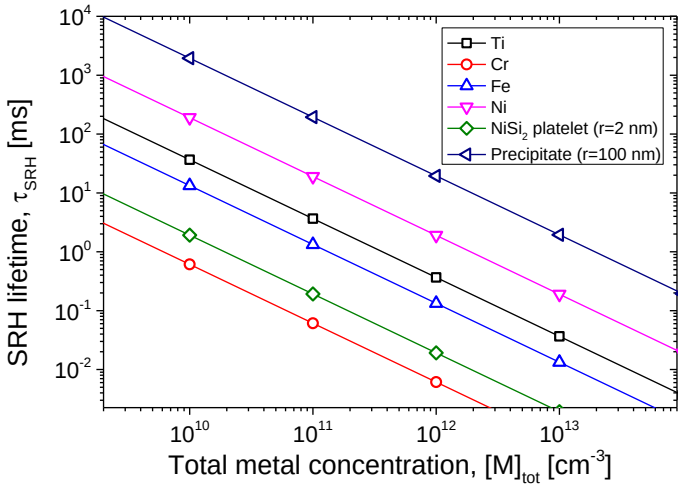

Figure 2. 1 Shockley-Read-Hall (SRH) lifetimes in p-type silicon (10^{16} cm^{-3} doping concentration) as a function of total metal concentration for different metals based on SRH parameters from Table 2. 5.

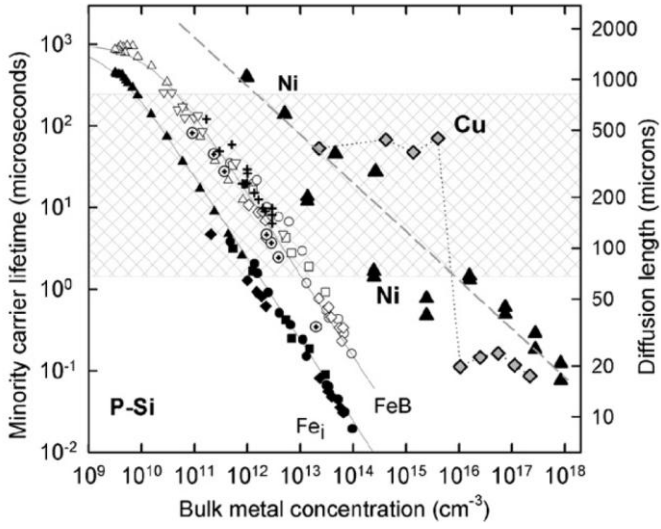

Figure 2. 2 Experimentally-observed degradation of minority carrier lifetime in p-type silicon as a function of bulk metal concentration, taken from reference [51].

The SRH lifetimes in p-type silicon as a function of various metal impurity concentrations are shown in Figure 2. 1. It is seen that Cr is the most detrimental

interstitial impurity followed by Fe, Ti and Ni. However, if Ni is precipitated as tiny silicide platelets, it is much more detrimental for the same total metal concentration. However, large precipitates are certainly more benign compared to tiny precipitates and interstitial impurities.

Istratov *et al.* have studied experimentally the lifetime degradation of p-type silicon as a function of different concentration of Fe, Ni and Cu [51] as shown in Figure 2. 2, which indicates that Ni and Cu are much more benign compared to Fe.

In the famous Westinghouse study [52], single crystalline silicon ingots intentionally contaminated with various metals were grown using the Czochralski method and solar cells were fabricated out of them. The resulting normalised efficiencies as a function of metal concentration for different metals are shown in Figure 2. 3, re-plotted with different colours by Pizzini [13]. Clearly, for each metal, beyond a threshold concentration, there is a steep drop-off in efficiency. Furthermore, the metal impurities appear to be bunched together in 3-4 groups. All 4*d* and 5*d* transition metals can only be tolerated at extremely low concentrations of < 10^{12} cm^{-3}. With the exception of Ti, the other 3*d* transition metals can be tolerated to much higher concentrations. Copper and nickel are the most benign metal impurities.

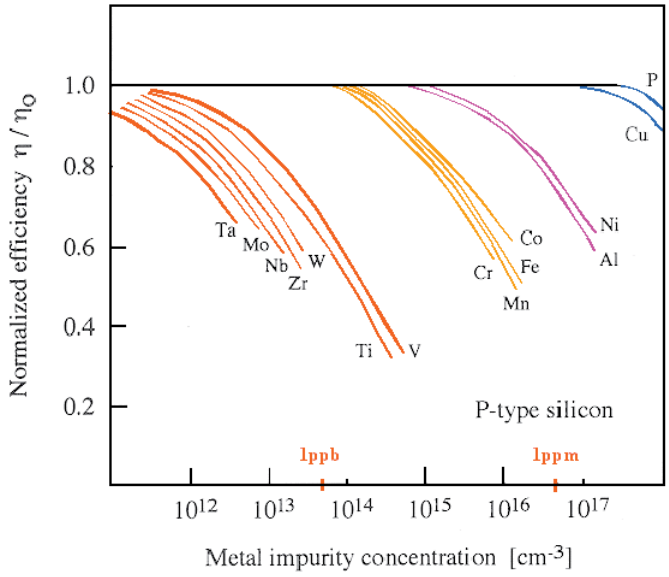

Figure 2. 3 The Westinghouse experiments showing the degradation of normalised efficiency of p-type silicon solar cells as a function of the metal impurity concentration reported first in [52] *and re-plotted by Pizzini et al. in* [13].

Similar work in multi-crystalline wafers was performed by Geerligs et al. [53], Dubois et al. [54] and Coletti et al. [55]. A similar degradation was also seen but the tolerance to metal contamination in multi-crystalline wafers seemed to be higher than mono-crystalline wafers [54], [55]. This has been attributed to internal gettering by grain boundaries which is not possible in mono-crystalline wafers.

Generally, the trend seen in Figure 2. 1 in the SRH lifetimes agrees with the Westinghouse experiments as seen in Figure 2. 3, but some important exceptions

and deviations can be noted. Firstly, titanium appears to be far worse than all other 3*d* transition metals in Figure 2. 3. Secondly, there is a large gap between Ni and the group of Cr, Mn, Fe and Co. A similar gap also exists between Ni and Cu. This can be explained by the fact that copper is an extremely fast diffuser, as is nickel to lesser extent. Titanium is a relatively slow diffuser. Thus, it can be anticipated that during the solar cell processing, metals such as Cu and Ni have a much higher likelihood to be gettered to surfaces or emitter regions and thus tolerated at much higher initial concentrations. Thus, diffusivities and solubilities of the metal impurities in silicon play an important role.

Diffusivity and solubility of transition metal impurities in silicon

The diffusivity, D_M, and solubility, S_M, of a transition metal impurity, M, at temperature, T, is given by [41]

$$D_M = D_0 \mathrm{e}^{-\frac{Q}{k_B T}} \tag{2.8}$$

$$S_M = S_0 \mathrm{e}^{\left(\frac{\Delta S_S}{k_B} - \frac{\Delta H_S}{k_B T}\right)}, \quad \text{for } T < T_{eut} \tag{2.9}$$

where Q is the activation energy for the thermally-activated jumps over potential barriers during diffusion, ΔS_S and ΔH_S are the solution entropy and enthalpy, respectively, associated with transferring one metal atom from the silicide phase to the silicon interstitial solid solution. k_B is the Boltzmann constant and T_{eut} is the eutectic temperature. D_0 and $S_0 = 5 \times 10^{22}$ cm^{-3} are pre-exponential factors. The values of D_0, Q, ΔS_S and ΔH_S for different metal impurities are given in Table 2. 6. The diffusivities and solubilities at the temperature of epitaxy i.e. 1130 °C is also given for all the metals[2].

Table 2. 6 The different constants of eqns. (2.8) and (2.9), namely D_0, H_M, S_S and H_S for different metal impurities in silicon are listed based on [41], [56].

Metal	D_0 [cm$^2 s^{-1}$]	Q [eV]	D_M [cm$^2 s^{-1}$] at 1130 °C	$\frac{\Delta S_S}{k_B}$	ΔH_S [eV]	S_M [cm^{-3}] at 1130 °C
Ti	1.45×10^{-2}	1.79	5.40×10^{-9}	4.22	3.05	3.77×10^{13}
Cr	1.0×10^{-2}	0.99	2.78×10^{-6}	4.7	2.79	5.24×10^{14}
Fe	1.3×10^{-3}	0.68	4.69×10^{-6}	8.2	2.94	5.02×10^{15}
Ni	2.0×10^{-3}	0.47	4.10×10^{-5}	3.2	1.68	(1.13×10^{18})
Cu	4.7×10^{-3}	0.43	1.34×10^{-4}	2.4	1.49	(2.45×10^{18})
B	5.1	3.7	2.62×10^{-13}			

Based on the values given in Table 2. 6, the diffusivities and solubilities of the different metals as a function of temperature are plotted in Figure 2. 4 (a) and (b) respectively. In order to put the diffusivities of the transition metals in perspective, the diffusivity of boron is also included. Even the slowest of the transition metals plotted, titanium, has orders of magnitude higher diffusivity compared to boron,

[2] For nickel and copper, the solubility values given in Table 2.6 are strictly-speaking invalid because T_{eut} for nickel and copper in silicon are 993 °C and 802 °C, respectively.

which is considered to be a fast-diffusing dopant species. Interestingly, the trend in the diffusivities seems to be similar to that seen in Figure 2. 3, suggesting that indeed the diffusion coefficients of metals play on important role not only in spreading contamination but also for gettering processes. The stark difference in the diffusivities between Ti and Fe/Cr is probably the reason why Ti is more detrimental for the solar cell characteristics compared to Fe/Cr, which were probably more easily gettered during the cell processing.

A similar trend is also observed for the solubility of transition metals in silicon with nickel and copper having much higher solubilities compared to the other transition metals. Thus, even though, for example nickel has higher diffusivity (which will aid gettering to surfaces for example) and smaller carrier capture cross-sections, its higher solubility allows a higher concentration of nickel to remain in the lattice during cool-down compared to a transition metal with lower solubility at the same temperature. Thus, a higher concentration would eventually remain in the active regions, which in the form of precipitates could be very harmful for minority carrier diffusion lengths.

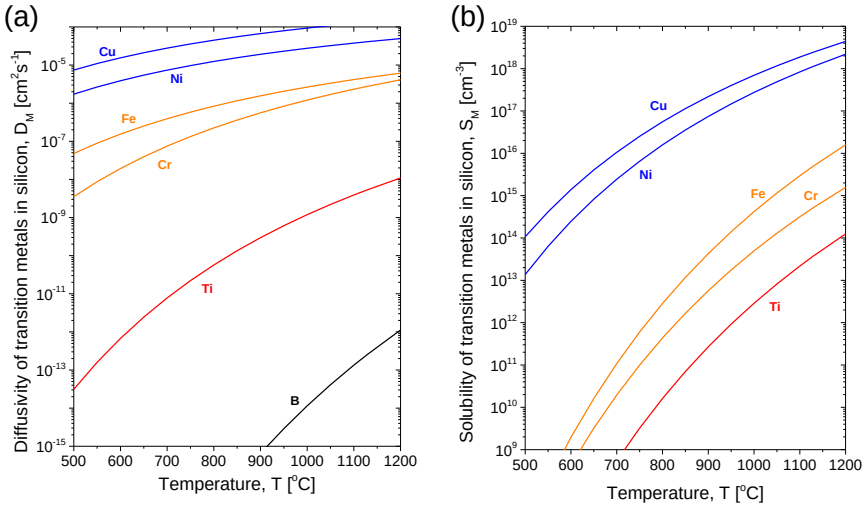

Figure 2. 4 Diffusivity and Solubility of different transition metals in silicon for a range of temperature, plotted based on Table 2. 6. Note that the plot involves extrapolation outside the range of temperatures for which the data in Table 2. 6 are valid.

Putting all of this in the context of WE-epicells, where an electronic grade epitaxial silicon layer is grown on low-quality substrate material, contamination of the epitaxial layer occurs via diffusion of mobile point defects from the substrate into the epitaxial layer. The precipitated metals in the substrate only act as sources of contamination by dissolving and replenishing the diffusing metal species leaving the substrate and entering the epitaxial layer. Therefore, the higher the diffusivity and solubility, the higher the possibility that the metal impurity in question will contaminate the epitaxial layer.

Based on this, it is expected that Ti is unlikely to be a dangerous impurity for WE-epicells due to low solubility and low diffusivity, even if the total metal concentration in the substrate is very high. However, metals such as Cu, Ni, Fe and

Cr will pose a significant threat to the minority carrier lifetime in the epitaxial layer. In the work of this thesis, particular focus will be placed on three metals, namely, Cu, Ni and Fe[3].

2.1.3 Specification for the metal contamination level in the substrate

From the discussions in the previous sub-sections, it is apparent that not all the impurities found in the feedstock ends up in the epitaxial layer. Thus, it is possible that orders of magnitude higher metal concentration in the initial feedstock can still lead to sufficient epitaxial layer quality.

The answer to the question of what is sufficient feedstock quality for a WE-epicell lies at the optimum point of the trade-off between cheaper silicon and higher power conversion efficiency. Geerligs *et al.* expressed the total production cost per watt-peak (W_p), $Co_{tot,ref}$, of a photovoltaic power conversion system based on a standard bulk silicon solar cell (with a power conversion efficiency, η_0), as the sum of material costs, area-related costs, Co_{area}, and area-unrelated costs, Co_{other} [53]

$$Co_{tot,ref} = m_{Si} P_{Si,ref} + Co_{area} + Co_{other} \tag{2.10}$$

where m_{Si} is the mass of solar-grade silicon feedstock used per W_p in a reference silicon solar cell including kerf loss. $P_{Si,ref}$ is the price of the reference solar-grade silicon feedstock per unit mass.

In the WE-epicell, a lower purity and therefore cheaper feedstock is used. Therefore, P_{Si} will be lowered. However, this would also mean a lower power conversion efficiency, η_{new}, which would require a greater mass of cheaper silicon per W_p. The area-related costs also increase due to the lower efficiency. In addition, the extra cost related to epitaxy, Co_{epi}, must be included. Thus, the new production cost, $Co_{tot,new}$ can be expressed as

$$Co_{tot,new} = m_{Si}\left(\frac{\eta_0}{\eta_{new}}\right) P_{Si,new} + \left(\frac{\eta_0}{\eta_{new}}\right) Co_{area} + Co_{other} + Co_{epi} \tag{2.11}$$

The closer $\eta_{new}$is to η_0, the more viable the concept of WE-epicells will be. Detailed cost calculations have not been done as part of this thesis. However, towards the goal of achieving high efficiencies with low cost feedstock, an inexpensive gettering layer in the form of an intermediate porous silicon layer is used in WE-epicells fabricated at IMEC, so that epitaxial layer contamination is strongly mitigated. Using such a gettering layer would allow further relaxation in the specification for the quality of the substrate.

A metal contamination specification for the feedstock of the substrate can be derived based on the above economic trade-off, whereby an average efficiency η that is needed to achieve a reduction in the production cost, Co_{tot}, is determined. Based on this, the minimum required bulk lifetime in the epitaxial layer can be determined, for instance, by modeling. This, however, intrinsically assumes that by

[3] Chromium is not studied because of restrictions on the type of metal element that can be annealed in certain clean room processing tools. Moreover, it is similar to iron in terms of diffusivity, solubility and recombination activity.

modulating feedstock quality, efficiencies close to that of a standard bulk silicon solar cell can be achieved. Brendel *et al.*, however, showed that for a high-efficiency WE-epicell, the open circuit voltage and therefore the efficiency, are limited by the interface recombination velocity at the high-low junction [28].

Thus, we can arrive at a specification for the efficiency (or epilayer bulk lifetime) by aspiring for an efficiency (or epilayer bulk lifetime) with a lower quality substrate such that the WE-epicell is not limited by bulk recombination. For this, a bulk diffusion length that is an order of magnitude higher than the thickness of the epitaxial layer must be targeted [57], which means for an epitaxial layer of 20-25 µm, a target bulk diffusion length is 200-250 µm. This corresponds to ~15-20 µs.

The epitaxial layer bulk lifetime specification, τ_{spec}, is associated with a maximum allowable metal contamination level for the metal impurity M in the epitaxial layer, $[M]_{epi}^{spec}$. In turn, this is then associated with a maximum allowable metal contamination level in the substrate, $[M]_{sub}^{spec}$, taking into account the thermal budget of the solar cell process flow, the accompanying metal diffusion processes, the diffusivities and solubilities of the metal impurities and gettering efficiencies of any gettering processes used. Finally, from this, the maximum allowable metal contamination level in the feedstock, $[M]_{feed}^{spec}$ can be found by considering the metal segregation in the melt during the crystal growth process. All of these are shown schematically in Figure 2. 5.

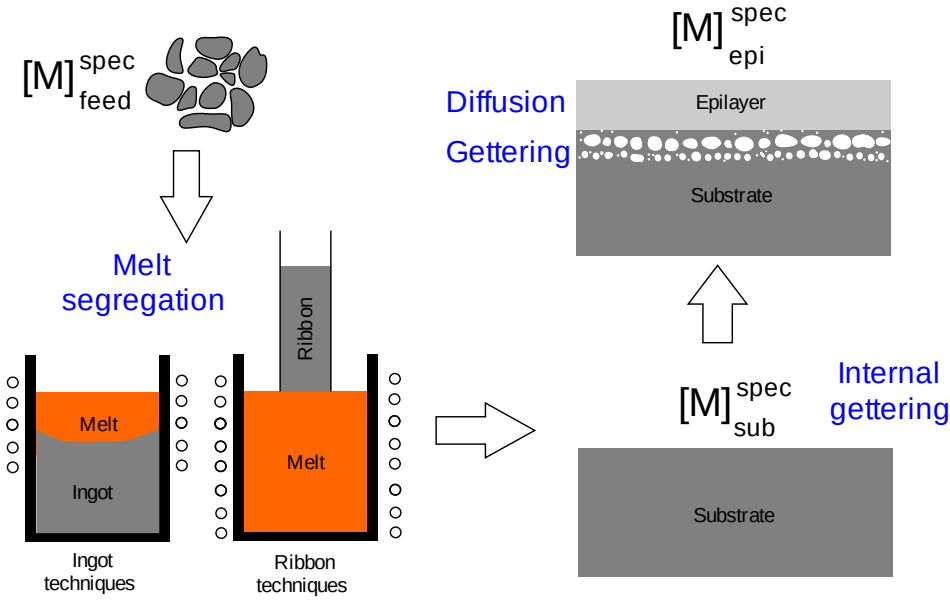

Figure 2. 5 The evolution of metal contamination level from feedstock to the epitaxial layer, highlighting processes that affect the metal concentration in the eventual epitaxial layer.

Assuming that the LLI bulk lifetime of the epitaxial layer is limited by metal contamination, we can express the relationship between τ_{spec} and $[M]_{epi}^{spec}$ as the sum of contributions from each metal type, in both interstitial and precipitated form i.e.

$$\frac{1}{\tau_{spec}} = \sum_{M} [M_i]_{epi}^{spec}\ \sigma_M v_{th} + 4\pi r_0 D_n N_{pre}^{spec} \tag{2.12}$$

$$[M]_{epi}^{spec} = [M_i]_{epi}^{spec} + N_{pre}^{spec} n_M \tag{2.13}$$

where $[M_i]_{epi}^{spec}$ is the maximum tolerable interstitial metal concentration for impurity M, N_{pre}^{spec} is the maximum tolerable metal precipitate density and n_M is the average number of metal atoms per precipitate. The other symbols have their usual meanings as defined before. The subscript "*i*" denotes "interstitial" metal impurity. Thus, the specification for the maximum metal concentration for each metal impurity depends also on the concentration of the other impurities either in interstitial or precipitated form. However, considering only one of the impurities and assuming it to be the dominant recombination centre, we can get the order of magnitude that is tolerable for each type of metal impurity.

The metal impurities found in the epitaxial layer come from diffusion of mobile metal impurities in the substrate. In contrast, the metal precipitates, typically in the form of metal silicides, in the substrate serve as sources to replenish the diffusing mobile metal impurities. Assuming the population of mobile metal impurities in the lattice is in equilibrium with the silicide precipitates in the substrate, the concentration of mobile impurities in the substrate, $[M_i]_{sub}$ is directly given by the solubility of the particular metal at the temperature in consideration (eqn. (2.9)). This would be the case for metals with low solubilities. However, if the total metal concentration in the substrate, $[M_{tot}]_{sub}$, is lower than the solubility limit, assuming the kinetics of silicide dissolution is fast enough and there is no internal gettering at high temperatures, then $[M_i]_{sub}$ will be given by the total metal concentration (i.e. complete dissolution). The subscript "*tot*" is used to refer to the total metal concentration which includes mobile interstitials and immobile precipitates. In equations, the above can be expressed as follows

$$[M_i]_{sub}(T) = \begin{cases} S_M(T) & \text{if } [M_{tot}]_{sub} > S_M(T) \\ [M_{tot}]_{sub} & \text{if } [M_{tot}]_{sub} < S_M(T) \end{cases} \tag{2.14}$$

In the WE-epicell process flow, the step with the largest thermal budget is the epitaxy itself which occurs at 1130 °C for 5-10 min depending on thickness of the epitaxial layer. The diffusion length during a high temperature process step for metal impurity M, L_{diff}^{M}, is given by $L_{diff}^{M}(T) = \sqrt{D_M(T_p)t_p}$, where $D_M(T_p)$ is the diffusivity of metal impurity M at process temperature T_p and t_p is the duration of the process step. The typical L_{diff}^{M} of various metals at the epitaxy temperature for different times are shown in Table 2. 7.

Thus, in the absence of gettering, we can expect metals such as Cr, Fe, Ni and Cu to distribute uniformly throughout the epitaxial layer and attain a concentration equal to $[M_i]_{sub}(T)$ given by eqn. (2.14). This completely ignores out-diffusion to the surfaces which could be important, particularly for metals such as nickel and copper. On the other hand, slow diffusers such as Ti are unlikely to affect epitaxial layers significantly. Although the diffusion length of Ti in Table 2. 7 is large enough compared to the thickness of an epitaxial layer (20-40 μm), the solubility of Ti is much lower and the rate of dissolution of precipitates replenishing the mobile Ti

supply is also much lower. This is because the characteristic time associated with the dissolution, τ_{sol}, given by, $\tau_{sol} = (4\pi r_{pre} N_{pre} D_M)^{-1}$ depends on D_M, the diffusivity of the interstitial metal impurity [58].

Table 2. 7 The diffusion length of different metal impurities at 1130 °C for different durations.

Metal	$L_{diff}^{M} = \sqrt{D_M(1130\ ^{o}\mathrm{C})t_p}$ [μm]		
	$t_p = 5$ min	$t_p = 10$ min	$t_p = 20$ min
Ti	13	18	25
Cr	290	410	580
Fe	380	530	750
Ni	1110	1570	2220
Cu	2010	2840	4010

However, if there is a gettering layer, such as porous silicon, in the WE-epicell structure with a gettering efficiency (defined as the ratio of gettered metal concentration and the lattice metal concentration), η_{gett}, then the concentration of mobile metal impurities would be reduced a factor equal to the gettering efficiency. Thus, we can express the maximum allowable metal concentration in the substrate for impurities with high solubility and diffusivity as

$$[M]_{sub}^{spec} = \begin{cases} [M]_{epi}^{spec} & \text{if there is no gettering} \\ \dfrac{[M]_{epi}^{spec}}{\eta_{gett}} & \text{if there is gettering} \end{cases} \tag{2.15}$$

Finally, the amount of metal impurities in the substrate depends on how efficiently the metal impurities are segregated into the melt during crystallisation. This depends on the growth method, the crystallisation speed, the volume of the remaining melt during crystallisation as well as the diffusivity of the metal impurities [59]. In general, this is well described by the Scheil equation given earlier (eqn. (2.1)), where $k_{eff,M}^{CG}$ depends on the parameters mentioned above. Thus, the maximum allowable metal contamination level in the feedstock is given as

$$[M]_{feed}^{spec} = \frac{[M]_{sub}^{spec}}{k_{eff,M}^{CG}(1-f_s)^{k_{eff,M}^{CG}-1}} \tag{2.16}$$

Based on the procedure explained in this section, and together with the specified assumptions, the metal contamination specifications required for the epitaxial layer, the substrate and the feedstock (used in directional solidification) in order to attain a 20 μs bulk lifetime in the epitaxial layer, is calculated and shown in Figure 2. 6 for different metal impurities, and for various assumptions about the gettering efficiency of porous silicon. The average concentration of most metals in UMG and MG silicon, based on Table 2. 2, are also indicated as a horizontal dash-dotted line. Note that iron concentration in MG silicon can be as high as 10^{20} cm^{-3}.

It is clear that the most detrimental of the considered impurities are iron and chromium, whose concentration in the eventual epitaxial layer cannot be higher than $\sim 10^{11}$ cm^{-3}. Titanium and nickel can be tolerated to much higher concentrations compared to iron and chromium. Titanium contamination in the epitaxial layer is limited by its low solubility and diffusivity. Copper, due to its high solubility was assumed to form precipitates in the epitaxial layer during the cool-down and was considered as such. Precipitates appear to be the most benign form of metal contamination which can be tolerated to $\sim 10^{14}$ cm^{-3}. This was also observed by Buonassissi, Istratov *et al.* [32], [51] who concluded that multi-crystalline substrates contain higher total metal concentration by virtue of precipitation in grain boundaries and crystal defects. Thus, a higher concentration can be tolerated.

Depending on the presence or absence of gettering and on the gettering efficiency, the specifications for the substrate and the feedstock vary as shown in Figure 2. 6. Even without any gettering whatsoever, significant concentrations of metals in the feedstock can still be tolerated, particularly if the metals end up in precipitated form in the epitaxial layer. However, MG silicon feedstock is too contaminated to be used for WE-epicells even with a highly-efficient gettering process with an efficiency of 10^3 incorporated into the cell process. Note that high concentration of Ti can be tolerated because the titanium contamination of the epitaxial layer is limited by its low solubility and low diffusivity.

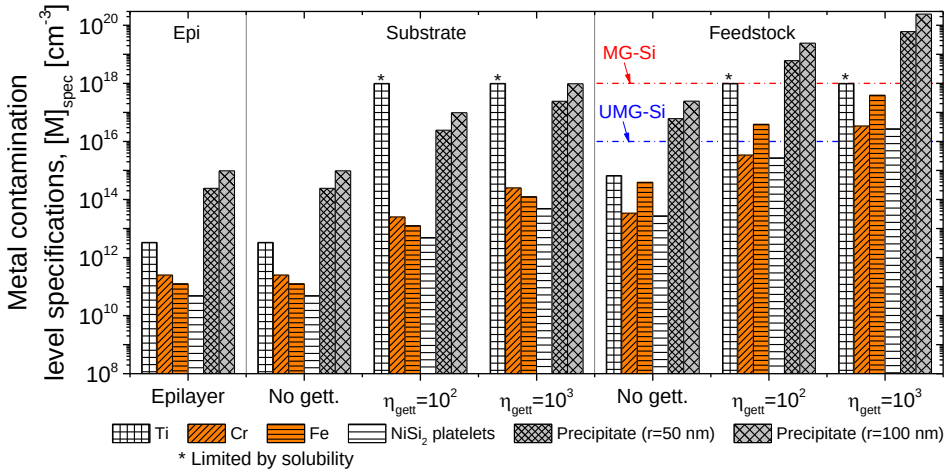

Figure 2. 6 Metal contamination specifications for the epitaxial layer, substrate and feedstock for a bulk lifetime specification of 20 µs, assuming for each metal impurity type that it is the limiting recombination centre. Metal impurities considered include Ti, Cr and Fe interstitials, Ni silicide platelets (r=2 nm) and large metal silicide precipitates (r=50 nm and 100 nm). Directional solidification has been assumed as the growth method with $k_{eff,M}^{CG}$ coming from Table 2. 1. f_s was assumed to be 0.5. Three different gettering efficiencies have been assumed for porous silicon. Horizontal lines at 10^{16} cm^{-3} and 10^{18} cm^{-3} are plotted to represent the average metal concentrations in UMG and MG silicon, respectively, as given in Table 2. 2. Note: for MG silicon, iron concentration can be as high as 10^{20} cm^{-3}.

On the other hand, UMG silicon with much lower metal concentrations can be used if a gettering process with a gettering efficiency of 10^2 for Fe and 10^3 For Cr and Ni can be implemented.

Thus, it is obvious that the incorporation of an efficient gettering is extremely important in order to relax the specifications for the metal contamination levels in the feedstock and thus the cost of a WE-epicell. In this chapter, particular focus will be placed on the detrimental and fast-diffusing metal impurities, namely iron, nickel and copper, in order to understand their gettering characteristics with respect to porous silicon.

2.2 Theory and modelling of transition metal gettering in porous silicon

From the previous section, the detrimental impact of the high solubility and diffusivity of transition metals in silicon was explained. For WE-epicells, it is of paramount importance to incorporate a highly efficient gettering layer such that high bulk lifetimes can be achieved in the epitaxial layers grown on low-cost substrates.

Metal gettering in solar cells is the process of removing detrimental metal impurities from active regions of the solar cell (source regions) to more thermodynamically-favourable locations (sinks) that lie outside the base regions, by means of diffusion processes. The sink regions must contain features which makes the interaction or segregation of these metal impurities energetically more favourable. Moreover, since diffusion is the main transport mechanism, gettering is performed at elevated temperatures so that metal impurities can be transported to the sinks efficiently. There has been extensive research over several decades on transition metal gettering in silicon by various groups. Due to this, gettering has been classified in various ways in literature, and with that various terminologies have been introduced depending on:

1. the gettering technique (e.g. aluminium gettering, phosphous diffusion gettering, HCl gettering, porous silicon gettering, etc.)
2. the gettering conditions (e.g. equilibrium or non-equilibrium gettering)
3. the gettering interaction (e.g. reaction-type or interaction-type gettering)
4. the gettering mechanism (e.g. relaxation gettering, precipitation gettering, segregation to second phases, trapping by atomic defects, etc.)
5. the gettering location (e.g. proximity gettering, internal gettering, external gettering, back-side gettering)

A comprehensive review of various gettering techniques used in the silicon microelectronics as well as photovoltaics industry, and the underlying mechanisms is given by Hieslmair, McHugo, Istratov and Weber in [60], [61] and by Myers [58], where the above terminologies have been explained. In this chapter, we will only concern ourselves with porous silicon gettering of transition metals, whose underlying mechanism is studied in detail in the forthcoming sections.

Porous silicon gettering in WE-epicells is implemented by a layer of annealed porous silicon at the interface between the low-cost substrate and the epitaxial layer, as explained in Chapter 1 and again depicted schematically in Figure 2. 7. This porous silicon layer, which also acts as a Bragg reflector, is electrochemically-etched in a HF-based electrolyte on top of the p^+ silicon low-cost substrate and sintered at a high temperature of 1130 ^oC to form voids or cavities with a diameter in the range of tens of nanometers. The quasi-monocrystalline surface of sintered porous silicon then acts as the template for the epitaxial growth which produces the active region of a WE-epicell.

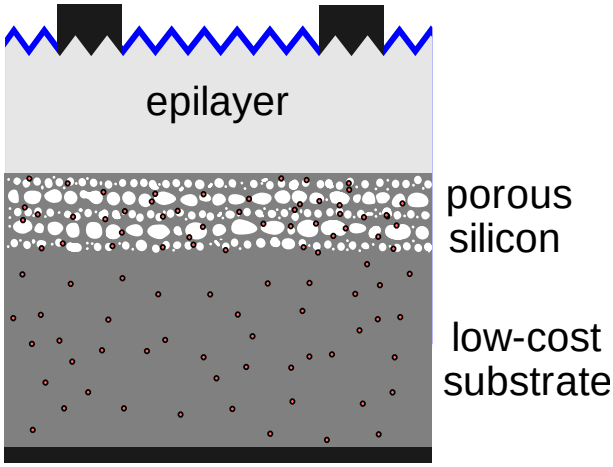

Figure 2. 7 Schematic of a WE-epicell, depicting the annealed porous silicon intermediate layer in between the low-cost substrate and the epitaxial layer. Porous silicon acts as a gettering layer to trap metal impurities, which would otherwise diffuse from the substrate and contaminate the epitaxial layer. The circles in the low-cost substrate depict metal atoms. Diagram is not drawn to scale or to proportion relative to the components

2.2.1 Equilibrium segregation of transition metal impurities in porous silicon

Nano-cavities with a diameter in the range of ~10 nm, created by high energy helium or hydrogen implantation and subsequent annealing, has been researched in 1990s by various groups as a promising technique for gettering transition metals in silicon wafers used in microelectronics fabrication [62]–[68]. Likewise, electrochemically-etched and annealed porous silicon as a gettering layer has also been investigated, albeit less extensively, by several groups for various applications [69]–[72].

Annealed porous silicon consists of voids in the range of 20-100 nm (depending on the initial porosity), whose surfaces act as thermodynamically-favourable sinks for the trapping of metal impurities. It has been shown that solute elements which decrease surface tension would segregate to the surfaces [73]. Atomistically, the lattice of silicon ends at the surface of these voids and thus presents a highly-disturbed configuration. Binding of metal impurities on these surfaces results in the liberation of free energy associated with the strain relaxation of the surfaces as well as passivation of dangling bonds, leading to the overall minimisation of free

energy of the system. The reduction of free energy of the system is in fact the driving force for porous silicon gettering.

The theory of grain boundary segregation of solute atoms in solid solution has been well-described in literature [73], [74] based on adsorption of gases on solid surfaces described by Langmuir. This theory can, in principle, be extended to porous silicon gettering, due to the similarity in the underlying physical mechanism.

The following derivation for porous silicon gettering is based on the theory of equilibrium metal segregation in grain boundaries as derived by McClean based on Langmuir-type monolayer adsorption [73]. Consider a silicon lattice with several voids such that P metal atoms are distributed among N silicon interstitial lattice sites, and p metal atoms are trapped among n void surface trap sites. For such a system in equilibrium, the minimisation of the Gibbs total free energy leads to the following relation

$$\frac{p}{n-p} = \frac{P}{N-P}\exp\left(\frac{\Delta G_B}{k_B T}\right) \tag{2.17}$$

where $\Delta G_B = \Delta H_B - T\Delta S_{v,B}$ is the free energy change associated with transferring a metal atom from a trap site to the interstitial site of the system. The free energy change includes both the change in enthalpy (ΔH_B) associated with the interaction energy between the metal atom and the void trap site, as well as change in vibrational entropy ($\Delta S_{v,B}$). Note that configurational entropy is already included in the derivation. This residual entropy change is however taken to be negligible assuming that the vibrational entropy does not change significantly. In other words, ΔG_B is taken to be the negative of the binding energy of a metal atom on a void surface trap site. In terms of fractional concentration, this can be expressed as

$$\frac{X_{void}}{X_{void}^0 - X_{void}} = \frac{X_{Si}}{1 - X_{Si}}\exp\left(\frac{\Delta G_B}{k_B T}\right) \tag{2.18}$$

where $X_{void} = p/n$ is the concentration of metal atoms trapped in the voids, $X_{Si} = P/N$ is the interstitial metal concentration in silicon and X_{void}^0 is the saturation level of X_{void}. k_B is the Boltzmann constant and T is temperature in kelvins. This equation is identical to the McClean model for grain boundary segregation [73].

There are several intrinsic assumptions in this derivation. Firstly, the metal concentration in the solid solution is assumed to be much lower than the solubility limit. Otherwise, the truncated BET theorem must be used to account for precipitation reactions [75]. For the work of this thesis, the gettering temperatures used are such that the metal concentrations are always much lower than the solid solubility limit and since fast quenching is done during experiments, the effect of precipitation reactions is kept to a minimum. Secondly, it has been assumed that the binding of one metal atom to a void surface trap site does not influence the binding of the metal atom in the neighbouring trap site. For weakly contaminated voids, this is a reasonable assumption. Finally, it has also been assumed that the gettering characteristics for one metal type (e.g. copper) is independent of that of another metal (e.g. iron). This is also reasonable for weakly contaminated voids.

By defining θ as the fractional coverage of the void surface trap sites, i.e. $\theta = \frac{X_{void}}{X_{void}^0}$, and assuming a dilute solid solution, the above equations can be transformed into

$$\theta = \frac{X_{Si}\exp\left(\frac{\Delta G_B}{k_B T}\right)}{1 + X_{Si}\exp\left(\frac{\Delta G_B}{k_B T}\right)} = \frac{1}{1 + \frac{1}{X_{Si}}\exp\left(-\frac{\Delta G_B}{k_B T}\right)} \tag{2.19}$$

The first expression for θ has the form of the Langmuir adsorption isotherm for gas adsorption on free surfaces [76], while the second expression has the form of a Fermi-Dirac distribution i.e. it gives the probability that a trap site on the void surface is occupied at a given temperature [77].

The fractional occupancy as a function of temperature is plotted for different binding energies as shown in Figure 2. 8. Gettering in a WE-epicell will take place during annealing and epitaxial growth at a temperature of 1130 °C. This temperature is also indicated in Figure 2. 8. The curves transit from an occupation probability of 1 at lower temperatures to 0 at very high temperatures, with the temperature of the sharp transition depending on the strength of the binding. Ideally, for efficient gettering, high temperatures are required so that diffusion processes are fast enough. Conversely, diffusion is the mechanism by which the epitaxial layer is contaminated by impurities from the substrate and a higher temperature would exacerbate this problem. However, high temperature is required for high quality epitaxy (lower crystal defects) and high growth rates (higher throughput). Thus, the use of high temperature is not a matter of choice. In order for porous silicon gettering to be already effective at such high temperatures, a binding energy associated with the interaction between a metal atom and a void surface trap site must be larger ≥2 eV.

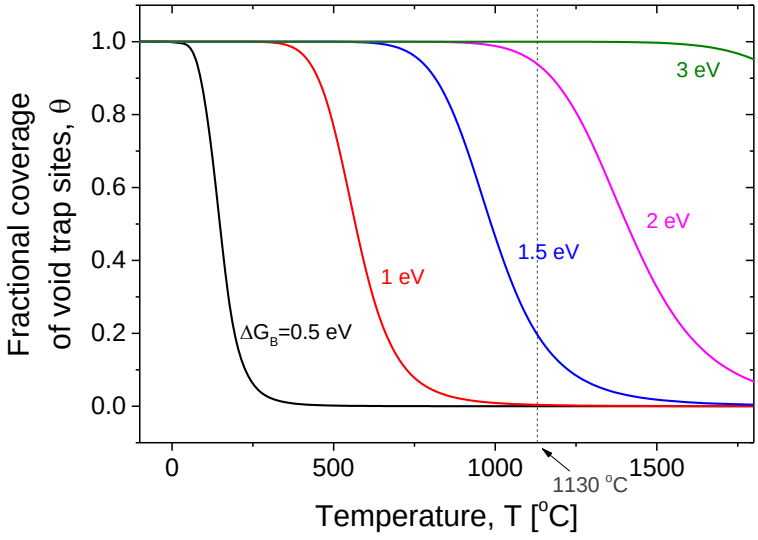

Figure 2. 8 Fractional coverage of the void trap sites as a function of temperature for different binding energies, calculated based on eqn. (2.19). The temperature at which epitaxy is performed is indicated by a vertical dashed line at 1130 °C.

For a dilute solid solution and weakly contaminated voids, eqn. (2.18) can be re-expressed as

$$\theta = X_{Si}\exp\left(\frac{\Delta G_B}{k_B T}\right) \tag{2.20}$$

Expressing eqn. (2.20) in terms of atoms per unit volume and re-arranging the terms, we obtain the gettering efficiency, which is defined as the ratio of concentration of trapped metal atoms to the concentration of mobile interstitial metal atoms in the silicon lattice, i.e.

$$\eta_{gett} = \frac{[M_T]_{void}}{[M_i]_{Si}} = \frac{[T]}{[Si]}\exp\left(\frac{\Delta G_B}{k_B T}\right) \tag{2.21}$$

where $[M_T]_{void}$ is the concentration of metal atoms trapped at void surfaces and $[M_i]_{Si}$ is the concentration of metal atoms that are still mobile in the interstitial locations of the surrounding silicon lattice. $[T]$ is the concentration of traps on the void surfaces, and $[Si]$ is the concentration of tetrahedral interstitial sites in the silicon lattice, which is equal to concentration of silicon.

The gettering efficiency as a function of different binding energies at three different temperatures is given in Figure 2. 9. Under equilibrium, the gettering efficiencies are obviously higher at lower temperature. At the temperature of epitaxy, a binding energy larger than 1.6 eV is sufficient to attain a gettering efficiency of 10^2, while a binding energy in the range of 1.9 eV and 2.2 eV are need to achieve gettering efficiencies of 10^3 and 10^4 respectively. Note that the gettering efficiency increases exponentially with a linear increase in the binding energy. It should be noted that the final gettering ratio will always be higher than predicted in Figure 2. 9 because segregation of metal atoms to trap sites will continue during the cool-down, so long as the diffusivities are large enough.

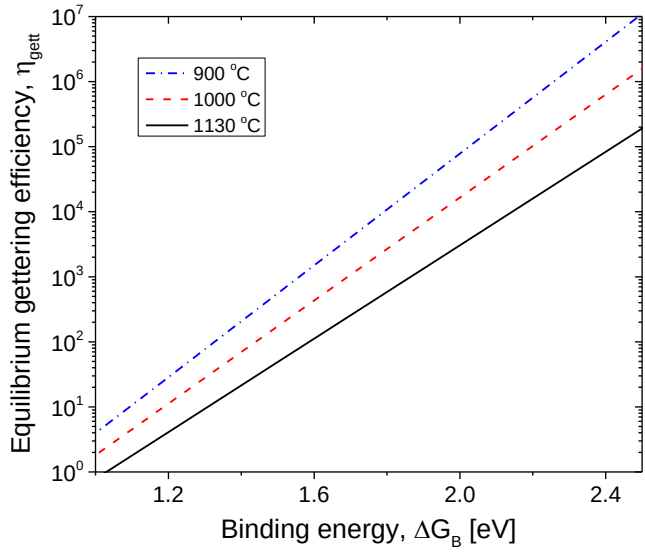

Figure 2. 9 Equilibrium gettering efficiency calculated based on eqn. (2.21) as a function of binding energy for three different gettering temperatures.

Finally, it should be stressed that the mechanism of porous silicon gettering is driven by the interaction energy of a metal atom with a void surface trap site without the formation of a second phase such as metal silicide. For silicide precipitation, super-saturation of the solid solution is a necessary condition and the final metal concentration in the silicon lattice will be limited to the solid solubility of the metal in silicon. In contrast, the gettering mechanism considered in this section proposes the formation of sub-monolayer of metal atoms on the void surfaces without silicide precipitation. This has been observed experimentally by Follstaedt *et al.* during gettering studies in implanted nano-cavities [65], [78]. In such a case, gettering is active at all metal concentrations, well below the solid solubility limit. This is an intrinsic advantage of this gettering technique.

2.2.2 *Ab initio* modelling of metal binding on void surfaces

From the understanding based on equilibrium thermodynamics, it is seen that the binding energy of a metal atom to a trap site on the void surface is an important parameter in determining the gettering efficiency achievable in porous silicon gettering for different metals. Efforts were made towards the calculation of binding energies from first principles and will be presented in this sub-section. This work was performed in collaboration with Newcastle University [79], [80].

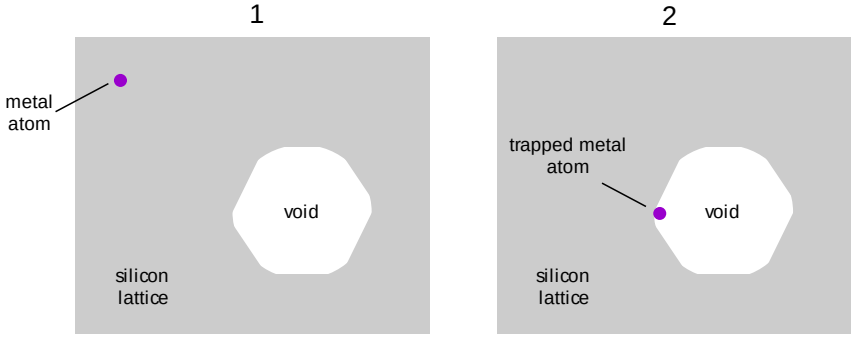

Figure 2. 10 Schematic depicting two systems comprising of a silicon lattice with a void. In system "1", which is the reference system, the metal atom is far removed from the void surface, while in system "2", the metal atom is placed at a trap site on the void surface. The difference in the total energy of the two systems is equal to the interaction between the metal atom and the trap site.

The binding energy associated with the trapping of a metal atom at a trap site on the void surface can be calculated by considering two systems as shown in Figure 2. 10. System "1" shows a void in a silicon lattice with a metal impurity atom "far away" from the void surface. This constitutes the reference system. System "2" shows the same structure but with the metal atom placed at a trap site on the void surface. The total energy associated with both systems will be different due to the interaction energy between the metal atom and trap site on the void surface. The difference in the total energy between these two systems will give the binding energy i.e.

$$E_B = E_{T,2} - E_{T,1} \tag{2.22}$$

where $E_{T,1}$ and $E_{T,2}$ are the total energy of the system "1" and "2", respectively and E_B is the binding energy. If the resulting $E_B < 0$, the binding interaction between the metal atom and the void surface trap site causes a reduction in the total energy and hence it will be favoured. If the total energy is increased, then the binding will be unfavourable.

The total energy of such systems can be calculated from first principles with atomic scale quantum mechanical modeling. Such *ab initio* simulations were performed using the Vienna *ab initio* simulation package (VASP) [81], [82] which is based on density functional theory (DFT) and plane-wave basis. Density functional theory is a formalism used to solve the many-body Schrödinger equation

$$\hat{H}\Psi_0(\boldsymbol{r_1}, \boldsymbol{r_2}, \dots, \boldsymbol{r_n}, \boldsymbol{R_1}, \boldsymbol{R_2}, \dots, \boldsymbol{R_N}) = E_0\Psi_0(\boldsymbol{r_1}, \boldsymbol{r_2}, \dots, \boldsymbol{r_n}, \boldsymbol{R_1}, \boldsymbol{R_2}, \dots, \boldsymbol{R_N}) \quad (2.23)$$

for the ground state by expressing the energy of the system, E, as a functional of the electron density, ρ, i.e.

$$E[\rho] = T[\rho] + V_{ee}[\rho] + V_{en}[\rho] \quad (2.24)$$

$\hat{H}$ is the Hamiltonian operator. Ψ_0 is the ground-state wavefunction which depends on the coordinates of the electrons, $\boldsymbol{r_i}$, and coordinates of the nuclei, $\boldsymbol{R_i}$. E_0 is the eigenvalue which gives the total energy of the system at ground state. $T[\rho]$, $V_{ee}[\rho]$ and $V_{en}[\rho]$ are energy functionals relating to the total kinetic energy, electron-electron interaction and electron-nuclei interaction, respectively. For the work of this thesis, DFT was used as a tool for calculating total energy of systems such as those depicted schematically in Figure 2. 10. For details of the DFT formalism, Capelle's introduction to DFT can be referred [83].

In our DFT simulations, void structures were created by taking a 512-atom silicon super-cell lattice and removing the atoms that are inside a sphere of a certain diameter to create a nano-void. Using two different radii, two different voids were created: a 29-atom nano-void with a truncated octahedral shape (V29) and a 35-atom nano-void with an octahedral shape (V35), as shown in Figure 2. 11 (a) and (b) respectively. Figure 2. 11 (c) shows the final super-cell consisting of a V29 nano-void in the middle of a silicon lattice consisting of 483 silicon atoms. These initial super-cells were geometrically optimised by fixing the silicon lattice constant and allowing the structure to relax such that the total internal force is less than 0.05 eV/Å.

In the relaxed void structures, all non-equivalent tetrahedral interstitial sites (T-sites) and substitutional sites (S-sites) were identified. Subsequently, metal atoms (copper or iron) were placed at the different T-sites or S-sites on the void surface as shown in Figure 2. 12 (a) and (b) respectively. For each case, the total energy was calculated using DFT. The generalised gradient approximation (GGA) was used to represent the exchange-correlation energy as described by Perdew and Wang (PW91) [84]. An energy cut-off of 250 eV was used for all the simulations and only Γ-point calculations were done, considering the large size of the super-cell. The resulting total energy was then compared to reference systems to calculate the binding energy for each site. For selected structures, a higher energy cut-off of 320 eV was used to test the convergence for energy cutoff and we found that the binding energy is valid with 0.2 eV error range.

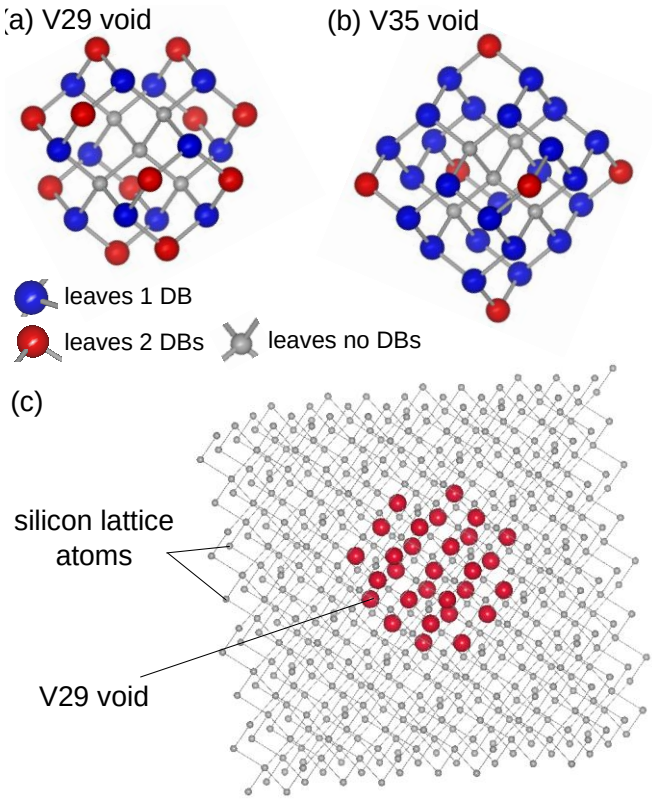

Figure 2. 11 Structure of the (a) V29 and (b) V35 voids, respectively. The number indicates the number of silicon atoms removed to create the void. The V29 void has a truncated octahedral shape while V35 void has an octahedral shape. The atoms depicted in (a) and (b) are colour-coded to indicate the number of dangling bonds (DBs) created upon their removal. Blue and red atoms result in the creation of 1 and 2 DBs respectively. (c) Structure of the final super-cell with a V29 void. The red spheres indicate the lattice locations of the void.

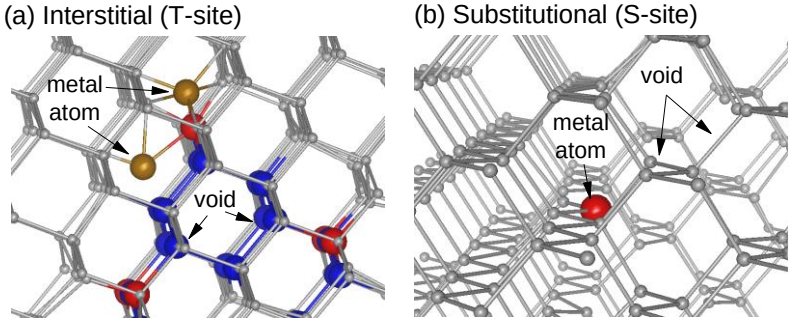

Figure 2. 12 (a) Atomic structure showing metal atoms placed at two different interstitial locations on the void surface. Note that in the actual DFT simulations, the binding of a metal atom to a surface site is tested one at a time. The red and blue spheres indicate lattice sites belonging to the void. (b) Atomic structure showing a metal atom placed at a substitutional site corresponding to a lattice site belonging to the void. In this case, the lattice points of the void are not shown. Bonds depicted between metal and silicon do not represent covalent bonds.

In practice, the binding energy is calculated as follows

$$E_B = E_{Si_{512-N}M} - E_{Si_{512-N}} - E_{Si_{512}M} + E_{Si_{512}} \quad (2.25)$$

where the energy terms on the right side of the equation are the total energy values obtained from different DFT calculations. N is the number of Si atoms removed to generate the void structure. $E_{Si_{512-N}M}$ corresponds to the total energy of a void structure containing an N-atom nano-void with a metal atom at the void surface. $E_{Si_{512-N}}$ corresponds to the total energy of the same void structure without the metal atom. $E_{Si_{512}M}$ corresponds to the total energy a silicon lattice without a void, but with a metal atom at an interstitial space. $E_{Si_{512}}$ is the total energy corresponding to a 512-atom silicon super-cell.

The result of a converged DFT simulation is plotted in Figure 2. 13, which gives the electron density of the void structure, showing a copper atom bound to a trap site on the surface of a V35 void. The magnitude of the binding energy for copper binding at this trap site is ~2.2 eV. In several other sites, negative binding energy values were obtained, indicating favourable binding. The binding energies calculated from rigorous simulations at all non-equivalent surface sites of a V35 void structure for both copper and iron binding are summarised in Table 2. 8. However, the results of the DFT simulations on the smaller V29 void will be deferred to Chapter 4.

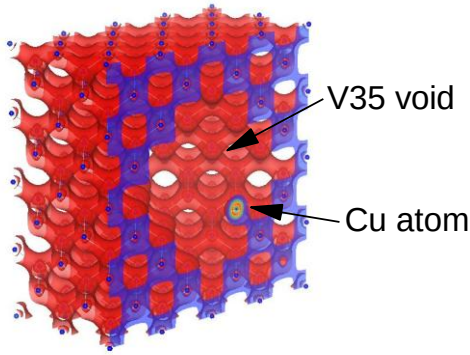

Figure 2. 13 Electron density plot of a void structure, containing the V35 void, obtained from a converged DFT simulation, showing a copper atom bound to a surface trap site.

Table 2. 8 Summary of the magnitude of the binding energies obtained from DFT simulations for iron and copper binding at V35 void surface sites. Experimentally-obtained values from literature are also given for comparison.

Metal	Magnitude of binding energy, $\|E_B\|$ [eV] from DFT calculations on V35 structures		Magnitude of binding energy, $\|E_B\|$ [eV] from literature
	Highest	Average	
Copper	2.28	2.07	2.2 [65]
Iron	2.18	1.83	1.5 [63]

The average binding energies obtained for iron and copper binding on the surface sites of the V35 void were computed to be ~1.83 eV and ~2.07 eV

respectively, which compares reasonably well with experimentally-found binding energy values from literature of ~1.5 eV and ~2.2 eV, respectively [63], [65]. Such high binding energies indicate that copper and iron will be gettered very effectively by porous silicon. From Figure 2. 9, this should result in a gettering efficiency of ~10^2-10^3 for iron and ~10^3-10^4 for copper.

2.2.3 Diffusion modelling of the distribution of metal impurities in an epitaxial structure

From the *ab initio* simulations, besides the average metal atom-void surface binding energies, the trap concentration can also be estimated by enumerating the sites where the metal atoms showed favourable binding. These parameters were then used in a diffusion model to study the time evolution of a uniform metal impurity profile in a structure with a porous silicon layer at high temperature. Figure 2. 14 shows an example of such a continuum simulation performed using the Sentaurus Process numerical simulator, which shows how the uniform initial Cu profile, with a concentration of 10^{15} cm^{-3}, evolves during 1 min of annealing at 1000^{o}C, corresponding to the growth of 1.3 µm of epitaxial silicon followed by a rapid cool-down to 900 ^{o}C. The binding energy in the porous silicon used for this calculation was 2 eV and the trap concentration was 10^{19} cm^{-3}.

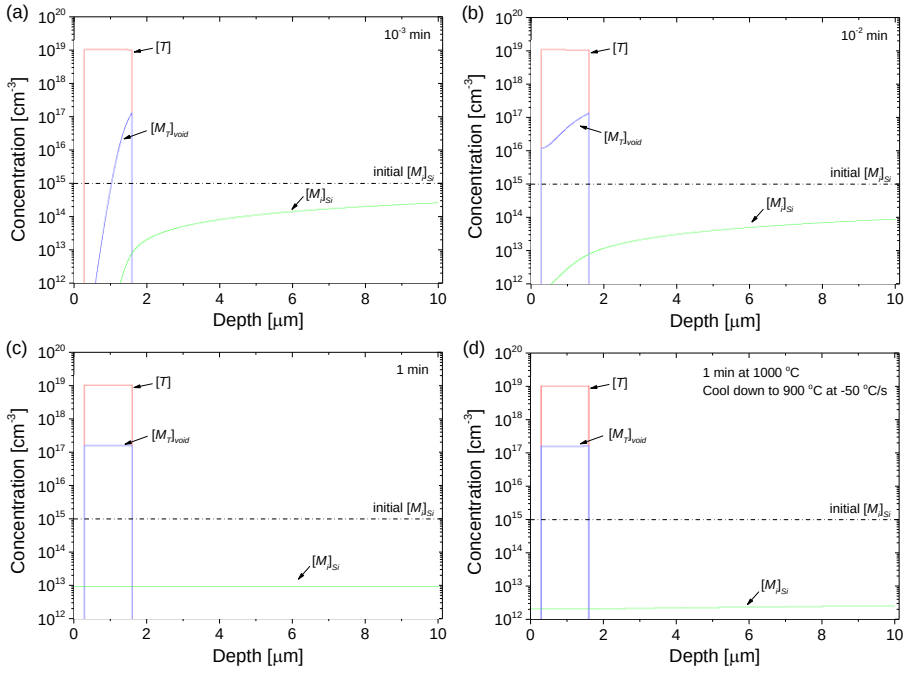

Figure 2. 14 Diffusion modelling using Sentaurus Process for an epitaxial p/p$^+$ silicon structure with an embedded porous silicon with a trap density, $[T]$, of 10^{19} cm^{-3} and an average copper binding energy of 2 eV. The initial $[M_i]_{Si}$ is 10^{15} cm^{-3}. The plots show the evolution of the trapped metal concentration, $[M_T]_{void}$ and the mobile metal concentration in the silicon lattice, $[M_i]_{Si}$ during an anneal at 1000 ^{o}C (a) after 10^{-3} min, (b) after 10^{-2} min and (c) after 1 min. (d) shows the profiles after 1 min of annealing at 1000 ^{o}C and a fast cool down to 900 ^{o}C at the rate of 50 ^{o}C s^{-1}.

During the high temperature treatment, there is a gradual build-up of copper in the porous silicon layer, and a concomitant depletion of copper elsewhere (Figure 2. 14 (a) to (c)). After 1 min, the system already attains equilibrium, as shown in Figure 2. 14 (c), due to the extremely high diffusivity of copper. The gettering ratio at 1000 °C is seen to be $\sim 10^4$, which corresponds very well with what was predicted by eqn. (2.21) and plotted in Figure 2. 9.

Interestingly, as the temperature is reduced during the cool-down from 1000 °C to 900 °C at a rate of 50 °C s^{-1}, there is further gettering of copper by the porous silicon and the $[M_T]_{void}/[M_i]_{Si}$ ratio reaches $\sim 10^5$. This, again, corresponds well with what is predicted by eqn. (2.21) for an equilibrium at 900 °C (see Figure 2. 9). Copper, being an extremely fast diffuser, attains equilibrium very quickly even during continuous cool-down.

In conclusion, due to the large binding energies associated with the interaction of metal atoms with the void surfaces, large gettering efficiencies can be obtained for porous silicon gettering of iron and copper.

2.3 Chapter summary

- The low-cost silicon feedstock options to fabricate low-cost substrates for WE-epicells include metallurgical grade (MG) silicon, upgraded metallurgical grade (UMG) silicon, "offspec/reject" silicon from the microelectronics industry as well as silicon "reclaimed" after stripping off the circuitry of used microelectronic devices.
- The most common metal impurities in low-purity feedstock are iron, nickel, chromium, copper and titanium.
- Among the low-cost crystallisation techniques discussed, directional solidification (DS), dendritic web growth and to an extent edge film-fed growth (EFG) and string ribbon (SR) are promising candidates.
- During crystallisation, purification of the silicon happens by means of melt segregation, given by the Scheil equation (eqn. (2.1)).
- Transition metal impurities in silicon exist as point defects or silicide precipitates.
- Transition metal impurities form defect states deep within the band gap of silicon. Thus, they are extremely efficient Shockley-Read-Hall (SRH) recombination centres for minority carriers in silicon.
- The low-injection SRH lifetime due to metal impurity point defects is inversely proportional to the metal concentration and the carrier capture cross-section of the metal impurity (eqn. (2.6)). The SRH lifetime due to metal impurity precipitates is inversely proportional to the precipitate density and precipitate radius (eqn. (2.7)). Among the considered metal impurities in p-type silicon, iron and chromium are the most detrimental and copper is the most benign. In general, the most recombination-active metal impurities are less detrimental when present in precipitate form.

- Transition metals have extremely high solubilities and diffusivities, with copper being the fastest and titanium the slowest among the $3d$ transition metals.
- Lower purity feedstock would lower the cost of the cell but also the efficiency. The trade-off is then an economical decision.
- A methodology for estimating the maximum metal contamination specification level for the feedstock and the substrate is presented which considers impurity segregation in melt during crystal growth, out-diffusion of impurities from substrate to epitaxial layer and a gettering scheme with different gettering efficiencies, η_{gett}.
- It is shown that it is possible to attain 20 μs bulk lifetime in the epitaxial layer with UMG silicon with porous silicon gettering. However, for MG silicon, the iron and chromium concentration would be too high, even when extremely efficient gettering processes are present. Porous silicon gettering allows the relaxing of the metal contamination specifications for the substrate and the feedstock.
- The theory of segregation of metal impurities at void surfaces is presented based on the McClean model for grain boundary segregation, which assumes a Langmuir-type surface chemisorption (eqn. (2.19)). A formula for the gettering efficiency is derived (eqn. (2.21)).
- *Ab initio* simulations using density function theory are performed to calculate binding energy of copper and iron atoms to void surface trap sites.
- Two void sizes are simulated: V29 and V35, where the number represents the size of the void in terms of number of silicon lattice vacancies.
- In V35 void simulations, large average binding energy values for iron and copper of ~1.83 eV and ~2.07 eV are obtained.
- This corresponds to a gettering efficiency of 10^2-10^3 for iron and 10^3-10^4 for copper at 1000 ^{o}C.
- Incorporating the binding energy and the calculated trap density in a diffusion model confirms the gettering ratios expected from theory.

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Chapter 3
Transition Metal Gettering by Porous Silicon: Experimental studies

In this chapter, the modeling results of Chapter 2 are verified experimentally through intentional metal contamination and gettering experiments on epitaxial structures. The gettering characteristics and gettering efficiency of porous silicon is evaluated using chemical and elemental analysis techniques (total reflection X-ray fluorescence and secondary ion mass spectroscopy) as well as minority carrier lifetime measurements.

3.1 Intentional metal contamination and gettering experiments

To verify the large gettering ratios predicted by modelling in the previous chapter, intentional metal contamination and gettering experiments were carried out. However, it is rather complicated to use low-cost substrates as experimental starting materials.

In typical low-cost substrates, the starting bulk metal contamination level is not known and must be analysed by chemical or elemental analysis techniques such as neutron activation analysis (NAA), graphite furnace atomic absorption spectroscopy (GF-AAS), or one of the different mass spectroscopy methods, namely inductively-coupled plasma mass spectroscopy (ICP-MS), glow discharge mass spectroscopy (GD-MS), secondary ion mass spectroscopy (SIMS) and secondary neutral mass spectroscopy (SNMS). Some of these techniques are discussed in [1].

Table 3. 1 shows the bulk metal concentration measured in four different UMG substrates using ICP-MS. Based on the significant variation in the metal content observed between the samples, it can be concluded that the metal concentration and the predominance of a metal type very much depends on the source of the ingot and feedstock used in the preparation of the low-cost substrates.

Table 3. 1 Bulk metal concentration (in ppmw) of different metals in four different UMG silicon substrates measured using ICP-MS in this work.

Impurity	Bulk metal concentration [ppmw]				
	Ti	Cr	Fe	Ni	Cu
UMG-1	0.246	0.0698	0.966	0.190	2.772
UMG-2	0.380	1.325	49.51	0.789	3.378
UMG-3	2.353	10.18	407.2	6.465	8.487
UMG-4	1.482	0.0765	1.988	0.0627	15.54

Moreover, the local distribution of the different metals and their form is also not known. For example, depending on the metal type, growth conditions and crystal quality, metals in the low-cost substrate could exist in the form of metal silicides or even oxides formed at defected locations in the substrate [2], [3]. Finally, due to the existence of grain boundaries and a generally large defect density in multi-crystalline substrates, competitive gettering effects could influence the evaluation of porous silicon gettering. All of these factors make low-cost substrates a complex system to use for dedicated porous silicon gettering studies. Therefore, gettering studies were done on high quality substrates, intentionally contaminated with known amounts of metal impurities.

Intentional metal contamination and gettering studies were carried out in epicell-like test structures, fabricated on 730 μm thick, mono-crystalline, 200 mm diameter, Czochralski (Cz)-grown p^+ wafers. These high quality, clean, single crystal silicon substrates act as model systems and allow porous silicon gettering to be studied in isolation of the effects outlined previously.

The general process flow used for the intentional contamination experiments is schematically shown in Figure 3. 1. Note that the process flow is formulated in such a way that metal contamination is introduced last in the process sequence[1], in contrast to real low-cost substrate where the metal contamination exists in the substrate prior to step 1 in Figure 3. 1.

In the middle of the 200 mm Cz wafers, an square-like 85 mm by 85 mm area of porous silicon is electrochemically-etched (step 1 in Figure 3. 1) in a hydrofluoric acid (HF)-based electrolyte (33% HF by volume in ethanol and water). Both the cross-sectional and top views are shown schematically in Figure 3. 1. In order to control the size of the voids in the porous silicon layer, the thickness and/or the porosity can be varied by altering the etch duration and etch current density. Typical thicknesses are in the range of 150 – 1500 nm and typical porosities in the range of 28-41%. The exact details will be given together with the results to be discussed later in this chapter. Following electrochemical etching, porous silicon is sintered at 1130 ^{o}C for 10-20 min in hydrogen ambient, which results in the formation of voids (step 2 in Figure 3. 1), as already explained in Chapter 1.

[1] This is because of strict regulations and restrictions regarding processing tool and sample contamination in the IMEC clean room. For example, metal contaminated samples are not allowed in the porous silicon tool, epitaxial reactor or the thermal oxidation furnace.

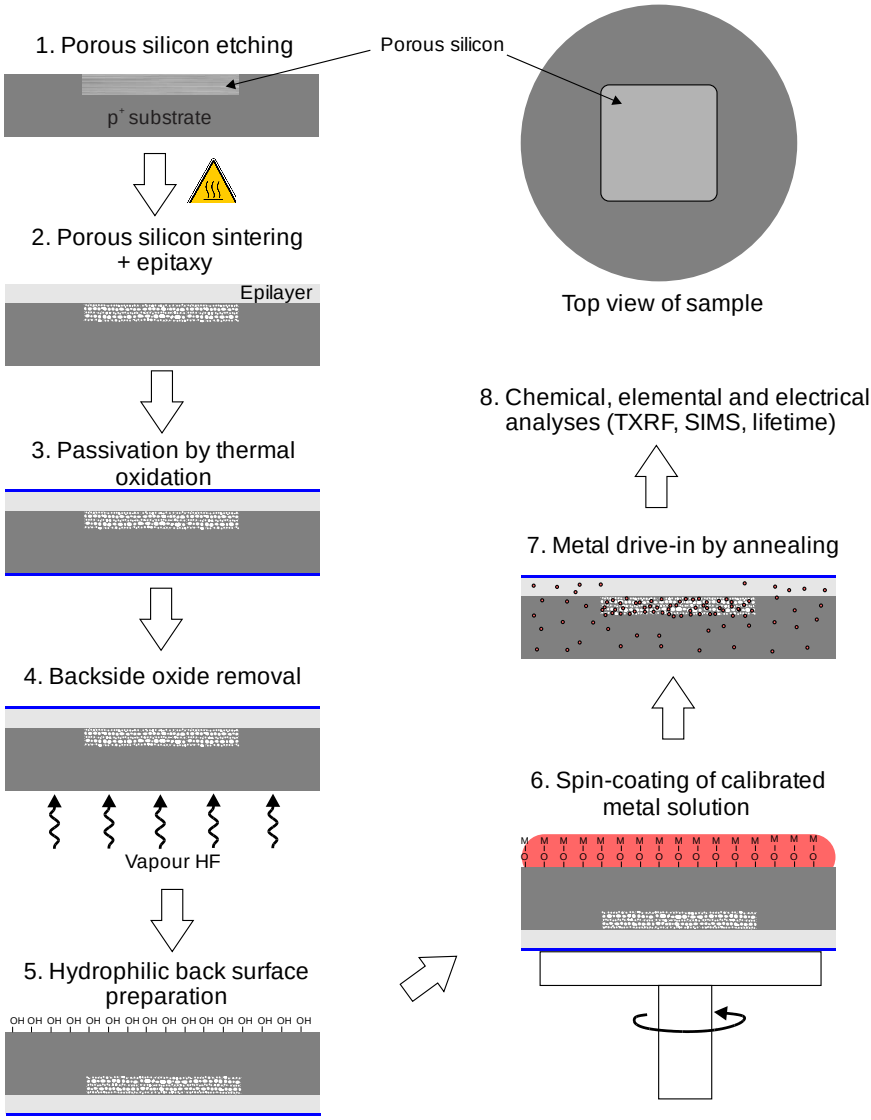

Figure 3. 1 Process flow used for intentional metal contamination and gettering experiments, formulated in such a way that metal contamination is introduced in the final steps of the sequence. Steps 3 and 4 are skipped for samples to be analysed by SIMS and TXRF. A top view of the sample after porous silicon etching is also given in the top right, showing that porous silicon is not present laterally everywhere. Note: proportions and dimensions are not to scale.

After this high-temperature reorganisation of the pores into voids, a p-type silicon epitaxial layer is grown *in situ* at the same temperature by atmospheric pressure chemical vapour deposition (APCVD) using trichlorosilane as the precursor gas. Here a distinction is made between samples used for chemical and elemental analysis, namely SIMS and total reflection X-ray fluorescence (TXRF) and those used for minority carrier lifetime measurements. For samples to be analysed by SIMS and TXRF, a 2 µm thick p^+ silicon layer with a boron doping concentration

of 1-2 $\times 10^{19}$ cm^{-3} is grown on top of the wafer, whereas for lifetime measurements, in addition to this p^+ silicon layer, a 25-50 μm thick p-type silicon layer with a boron doping concentration of 10^{16} cm^{-3} is grown. The p^+ silicon layer acts as a back surface field (BSF) to repel minority carriers electrons, as explained in Chapter 5 and 6.

Next, for the samples to be analysed by SIMS and TXRF, steps 3 and 4 in Figure 3. 1 are not needed and hence skipped. The samples for lifetime measurements are passivated by thermal oxidation (step 3 in Figure 3. 1) in a quartz boat furnace with dry oxygen at 1050 ^oC which forms a dense film of ~140 nm thick silicon dioxide. This silicon dioxide layer is not only an excellent surface passivation layer but also a good blocking layer for contaminants transported and delivered to the front surface of the wafer via gas phase (during step 7 in Figure 3. 1).

Now, in order to introduce metal contamination into the sample, the silicon oxide layer on the rear surface is etched using gaseous HF for 2-3 min at room temperature (step 4 in Figure 3. 1), in a configuration which only exposes the silicon dioxide on the rear surface. After silicon dioxide removal, the rear surface is hydrophobic with hydrogen-terminated silicon surface atoms. A hydrophobic surface is not amenable for spin-coating of contaminants contained in aqueous solutions.

Therefore, the wafer is treated in an ammonium hydroxide (NH_4OH)-hydrogen peroxide (H_2O_2) mixture (APM) constituting of (25% NH_4OH: 30% H_2O_2: water = 4:1:1) for 10 min at 80 ^oC to render the rear surface hydrophilic, with the surface silicon atoms having a hydroxyl (-OH) termination (step 5 in Figure 3. 1).

The back surface of the wafers is then contaminated by spin-coating metal solutions of pre-determined concentrations, prepared using standards calibrated against references from National Institute of Standards and Technology (NIST) of the U.S.A., as shown in step 6 of Figure 3. 1. During this step, the aqueous metal solution is poured onto the rear surface and allowed to stand for 40 s, during which metals in the solution react with the –OH groups on the surface i.e. $Si-OH + M^{n+} \rightarrow Si-OM^{(n-1)+} + H^+$ forming a chemical equilibrium [1 and references there-in]. After 40 s, the wafer is spun at a high speed to spin-off the excess liquid on the rear surface. During this step, a certain amount of metals will precipitate as salts on the wafer surface. Thus, besides the chemisorption of metals on the wafer surface, this precipitation also contributes to the final metal concentration at the back surface of the wafer.

This step is well optimised and calibrated empirically such that for a given metal concentration in the prepared metal solution and the spin-coating parameters, the resulting surface metal concentration is known. Figure 3. 2 is the TXRF map showing the surface copper concentration of a spin-contaminated sample with a target copper concentration of 10^{15} cm^{-2}. The result shows an average surface copper concentration of 9.1±2.2× 10^{14} cm^{-2}, which is reasonably close to the target concentration. The distribution of the copper across the wafer is largely uniform with slightly lower concentrations in the centre and the edges. Typical concentration used in the experiments range from 10^{12}-10^{15} cm^{-2}, and will be specified with the discussed results. The metals investigated include iron, nickel and copper.

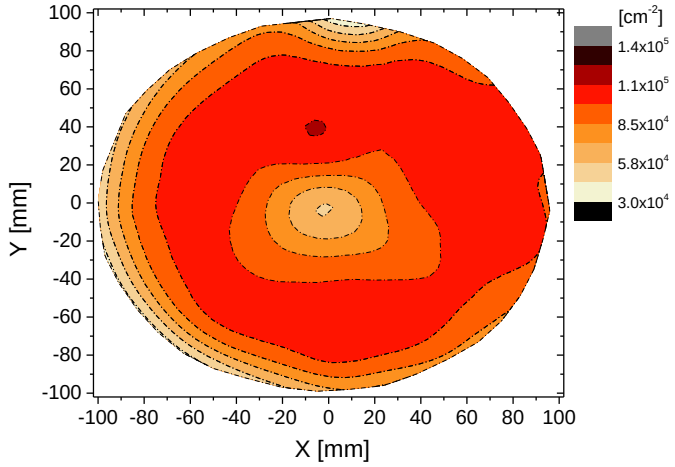

Figure 3. 2 TXRF map showing the surface copper concentration after a spin contamination with a target copper concentration of 10^{15} cm^{-2}. The average copper concentration is $9.1\pm2.2\times 10^{14}$ cm^{-2}.

After spin-contamination, the metals at the surface are driven in by a high temperature annealing step (900-1000 °C for 2-15 min, depending on the metal type) which will re-distribute the metals throughout the wafer (step 7 in Figure 3. 1). Two types of tools were used for annealing. For the samples for SIMS and TXRF analysis, a rapid thermal processing (RTP) tool was used, which has a fast temperature ramp rate. This allows the metal impurities to be quenched in as much as possible during the cool-down, after a high temperature anneal. For the samples for lifetime measurement, a quartz boat furnace was used with a much lower ramp rate.

Finally, the metal distribution in the samples are analysed using various techniques. Using a TXRF mapping measurement on the front side of the wafer, it will be possible to measure the amount of metal impurities diffusing through the entire substrate and reaching the top surface of the wafer. Using SIMS, the in-depth metal concentration in the porous silicon area can be measured. Finally, using minority carrier lifetime measurements, the epitaxial layer lifetime degradation due to the metal contamination in the presence/absence of porous silicon can be evaluated.

3.2 Chemical and elemental analysis of metal segregation in porous silicon

As described in Section 3.1, a sample containing a 1.5 µm thick porous silicon layer (with 28% porosity) was back surface-contaminated with a mixed metal solution (containing iron, nickel and copper) to a surface concentration of $\sim 10^{15}$ cm^{-2} for each metal and subsequently annealed at 950 °C for 15 min. During the anneal, the metal impurities at the back surface of the wafer will in-diffuse and distribute throughout the sample. We can expect, based on the modelling, that the

metal impurities will interact with the trap sites in porous silicon and tend to accumulate in the porous silicon layer. This also implies that the epitaxial layer on top of the porous silicon area should be less contaminated than that on top of pristine silicon.

3.2.1 Analysis of surface metal concentrations by TXRF

During the cool down, as the solubility reduces, in addition to porous silicon gettering, one may expect an out-diffusion of metal impurities in the sample to the front and back surfaces. This phenomenon can be used to probe the contamination level of the epitaxial layer. Where the epitaxial layer is less contaminated, less metals will out-diffuse to the front surface of the wafer. A direct TXRF mapping measurement at the front surface can be used to measure the surface metal concentration of all three metals across the wafer. The surface metal concentrations maps of all three metals (copper, nickel and iron) obtained from such TXRF measurements for the sample described above is shown in Figure 3. 3.

A square-like pattern in the middle of the wafer with very low surface concentrations for all three metal impurities is observed (Figure 3. 3 (a), (c) and (d)). This corresponds very well to the area where there is an embedded porous silicon (see top view schematic in Figure 3. 1), which was only etched in an 85 mm by 85 mm area confined in the middle of the wafer. As expected, the concentration of metals in the epitaxial layer on top of the embedded porous silicon layer is very low. In fact, in most of the points measured in the porous silicon area, the surface metal concentration was below the detection limits. On the other hand, the metal concentration outside the porous silicon area for all three metals are several orders of magnitude higher compared to that inside the porous silicon area. A control wafer without porous silicon shows no such pattern with uniform high copper surface concentrations. Comparing the three metals, the average metal concentrations in the periphery follows the order of diffusivity. Since copper is the fastest diffuser, more copper out-diffuses to the surface during the cool-down compared to iron, which is the slowest of the three metals.

Taking copper as an example, the drastic differences in the surface copper distribution is demonstrated using box plots, as shown in Figure 3. 3 (b), where three regions have been defined: (1) the porous silicon area contained within an 80 by 80 mm area in the middle of the wafer, (2) the periphery taken to be the area outside an 110 by 110 mm area defined in the middle of the wafer, and (3) the intermediate zone in between these two areas. The intermediate zone is an area which contains the peripheral regions of porous silicon that is not well-defined, areas of defected epilayer and regions where lateral gettering by porous silicon may be felt. The mean surface copper concentration in the periphery is seen to be $\sim 10^3$ times more compared to that in the area with embedded porous silicon, while lateral gettering is observed in the intermediate zone. This clearly demonstrates the strong gettering effect of porous silicon for all three metals. This is the first time the drastic influence of porous silicon on the epilayer contamination level has been unambiguously shown [4], [5].

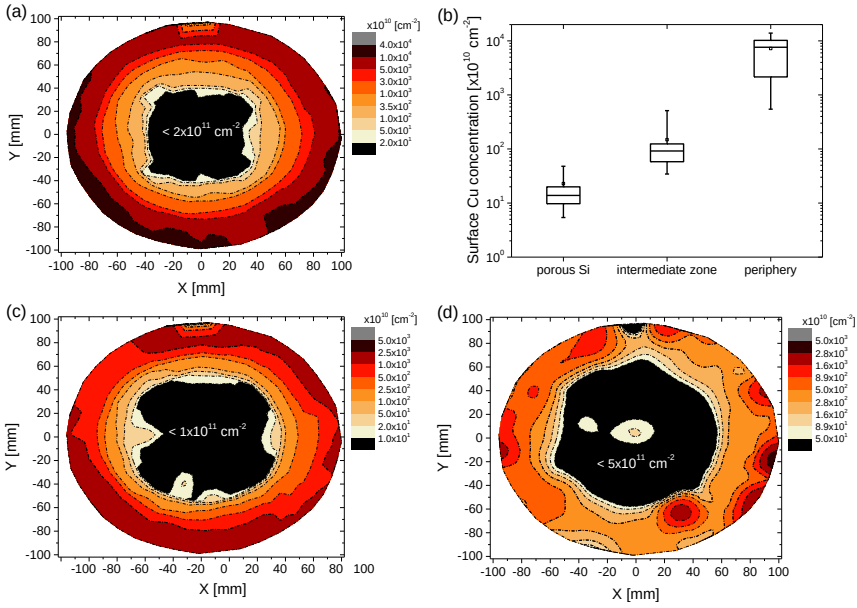

Figure 3. 3 Map of the surface metal concentration obtained by TXRF measurement on a sample that was back surface-contaminated to a concentration of ~10^{15} cm^{-2} and annealed at 950 ^{o}C for 15 mins, for (a) copper, (c) nickel and (d) iron. (b) Box plots of surface copper concentration in three different concentric areas, namely (1) porous silicon area, (2) intermediate zone, and (3) periphery.

3.2.2 Analysis of bulk metal concentrations by SIMS

Next, in order to evaluate if there is an accumulation of metals in the porous silicon, the metal concentration in depth in the porous silicon area is analysed using SIMS depth profiling. Two samples with a bilayer of porous silicon (200 nm of low porosity + 200 nm of high porosity as shown in Figure 3. 4) were surface contaminated with a mixed metal solution (containing iron, nickel and copper) and annealed at 1000^{o}C for 12 min. During cooling, two different nitrogen flow rates were used to investigate the effect of cooling rate on the metal profile within the sample.

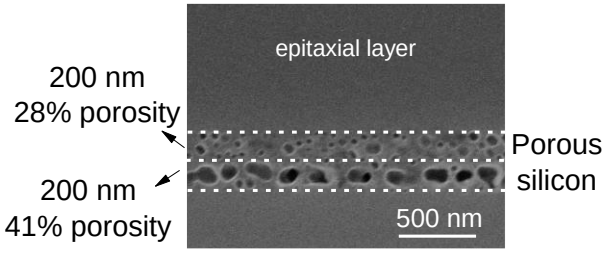

Figure 3. 4 A cross-sectional scanning electron microscopy (SEM) image showing the microstructure of the porous silicon stack consisting of two layers of different porosities, used in a gettering experiment.

The first sample was contaminated to a surface metal concentration of 5×10^{14} cm^{-2} and a slow cooling rate was used. The resulting metal concentration profiles in depth for all three metals are plotted in Figure 3. 5. All three metals show large peaks ($\sim 10^{18}$-10^{19} cm^{-3}) at a depth of ~2000-2400 nm. This corresponds precisely to the depth where porous silicon exists, indicating that there is a strong accumulation of iron, copper and nickel in the porous silicon layer. SIMS depth profiling on a control wafer without intentional contamination shows no such peak. The concentration levels in the bulk of the substrate and the epilayer as depicted are actually detection limits and the actual concentration is not known. Given that the peak concentration in the porous silicon is > 10^3 times the detection limits, the gettering ratio is at least $\sim 10^3$ for copper and nickel and $\sim 10^2$ for iron. This unambiguously further proves that porous silicon is an excellent gettering layer for copper, nickel and iron, as predicted by the modelling in Chapter 2. It is because of this strong gettering property of porous silicon that the contamination level in the epitaxial layer above porous silicon is much lower as deduced from the TXRF mapping results discussed earlier.

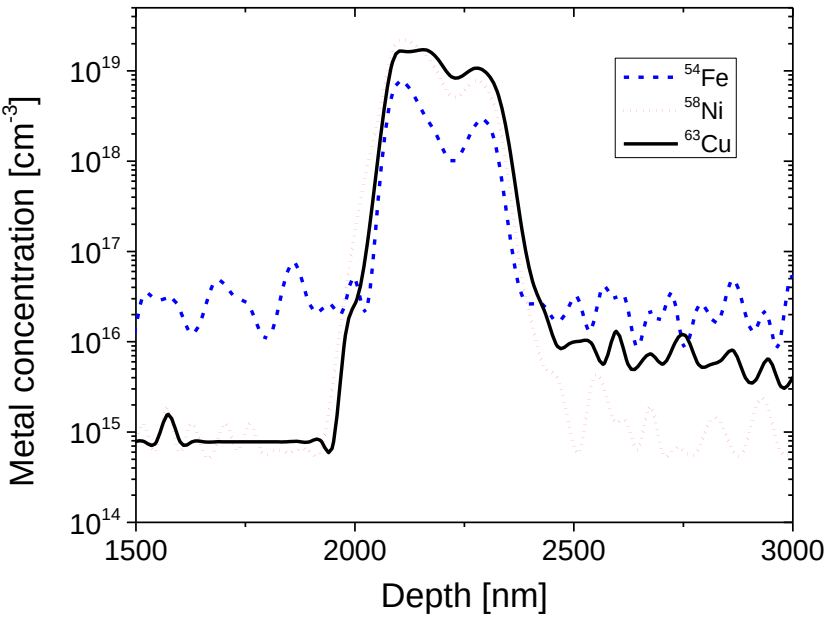

Figure 3. 5 Metal concentration profiles in depth obtained by SIMS depth profiling in an epilayer/porous silicon/substrate stack that was surface-contaminated with a mixed metal solution containing iron, nickel and copper to a surface concentration of 5×10^{14} cm^{-2} *and annealed at 1000 °C for 12 min. A slow cooling rate was used. Porous silicon stack has the structure shown in Figure 3. 4.*

While copper accumulation in porous silicon was already shown in epilayers grown on MG and UMG silicon substrates [4], [6], strong iron and nickel gettering by porous silicon is proven for the first time. Although iron gettering contrasts with the anomalous behaviour reported in [4], this result is consistent with the *ab initio* simulations of Chapter 2, Section 2.2.2 and the iron gettering by nano-cavities reported in [7].

Another important feature that can be observed in Figure 3. 5 is that the metal concentration peaks within the porous silicon layer consist of two sub-peaks, one higher than the other. This seems to be related to the fact that the porous silicon stack consists of two layers of different porosities (see Figure 3. 4). A higher metal concentration is observed in the low porosity (28%) layer compared to the high porosity (41%) layer. Further discussion on this is deferred to Chapter 4.

A second sample with the same porous silicon stack was contaminated to a surface metal concentration of 1×10^{14} cm^{-2} and a fast cooling rate was used this time. The resulting metal concentration profiles in depth for all three metals are plotted in Figure 3. 6. Similar to the previous sample, strong peaks are observed at the depth associated with porous silicon. However, a number of differences can be noticed.

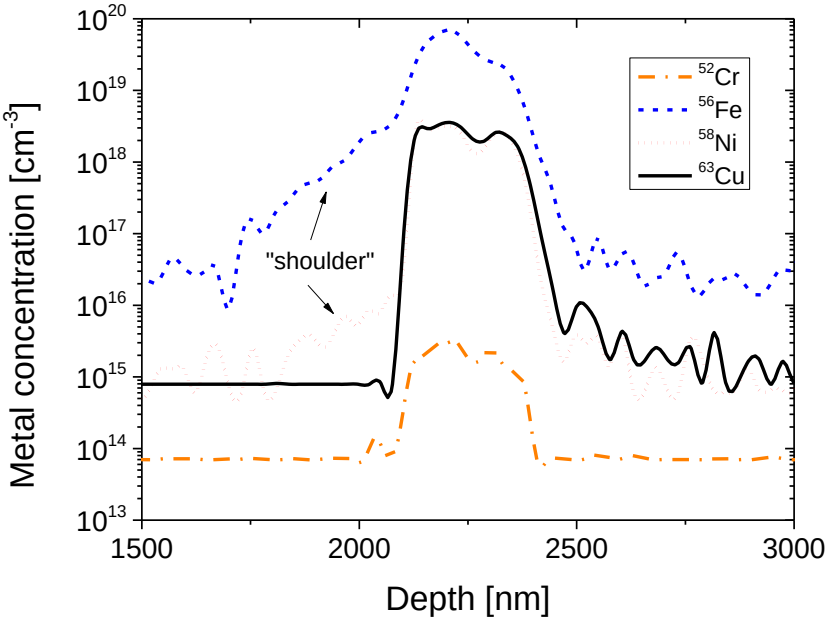

Figure 3. 6 Metal concentration profiles in depth obtained by SIMS depth profiling in an epilayer/porous silicon/substrate stack that was surface-contaminated with a mixed metal solution containing iron, nickel and copper to a surface concentration of 1×10^{14} *cm*$^{-2}$ *and annealed at 1000* ^{o}*C for 12 min. A fast cooling rate was used. Porous silicon stack has the structure shown in Figure 3. 4.*

Firstly, a "shoulder" of high concentration of iron and nickel can be clearly discerned at the interface region between the porous silicon layer and the epilayer. This is believed to be due to the existence of crystal defects at the interface such as misfit dislocations which can also getter metals. In fact, this "shoulder" does not exist for copper while that of iron is more pronounced compared to that of nickel. This follows the trend of their respective diffusivities with copper being the fastest and iron the slowest of the three elements. The rather large binding energies of metals to void surfaces allows porous silicon to already getter metal impurities at the high annealing temperature of 1000 ^{o}C, while the dislocations are inactive as gettering sites due to their lower binding energy of ~0.7 eV [8] (see Figure 2.8 in Chapter 2). However, as the

sample is cooled, dislocations become active gettering sites and compete with porous silicon to getter metal impurities. Upon further cooling, the solubility of the metals in the silicon is lowered, leading to supersaturation conditions for metals that did not already segregate to the void surfaces. In a fast cooled sample, these metals will quickly segregate to any energetically-favourable site, be it a void surface or a dislocation core, leading to the formation of this "shoulder" of high interfacial metal concentration. However, since copper has the highest diffusivity, no "shoulder" is observed because it is able to diffuse quickly enough to the porous silicon layer, whereas iron which is slowest diffuser of three metals investigated shows the largest "shoulder".

On the other hand, when the wafer is cooled slowly (see profiles in Figure 3. 5), the super-saturation of metals in the silicon matrix increases at a pace that gives sufficient time for all the three metals to getter to the most favourable locations i.e. the void surfaces. This is why the iron and nickel profiles in Figure 3. 5 show no such "shoulder" of high metal concentration at the interface when cooled at a slower rate.

Secondly, it is observed that the peaks of copper and nickel in Figure 3. 6 are slightly lower than that observed in Figure 3. 5. This is because the initial surface metal contamination is lower in the latter case. However, in contrast to nickel and copper, the iron peak is significantly larger despite a lower concentration of surface contamination used in the second sample. Moreover, the metal concentration is also higher than the trap density predicted in Chapter 2 to be $\sim 10^{19}$ cm^{-3}. These seem to indicate that there must be multi-layer segregation of iron at the porous silicon surfaces i.e. a precipitation-like reaction. This could be due to additional iron already present in the p^+ silicon substrate, prior to surface contamination. In support of the argument that there has been an additional source of contamination besides what was spin-coated on the wafer surface, a tiny peak is also visible for chromium for the second sample (see Figure 3. 6) but not found for the first sample. Chromium was detected despite not being introduced intentionally in the p^+ substrate.

There are two possible sources for this additional contamination. It could have either existed in the starting silicon substrate itself or it could have been introduced from the metal-contaminated annealing tool which was used for the metal drive-in. It is known that the supply of p^+ Cz silicon can vary in quality even within a batch and the wafers may contain some metal impurities. GD-MS measurements on "clean" p^+ Cz substrates presented in Chapter 6, Section 6.1.2 show presence of iron to a concentration of $\sim 2.0 \times 10^{14}$ cm^{-3}.

Thus, it is hypothesised that the additional iron, that was probably present besides what was intentionally introduced, resulted in a stronger super-saturation during cooling, leading to a stronger driving force for precipitation-like gettering processes.

3.3 Assessment of the quality of gettered epitaxial layers using lifetime measurements

From Section 3.2.2, it is quite clearly proven that porous silicon is an excellent gettering layer with a large gettering efficiency. However, with these chemical and elemental analyses techniques, it is not possible to probe the level of metal contamination in the epitaxial layer because the minimum detectable metal concentrations are rather high. For example, the detection limit for iron based on Figure 3. 5 and Figure 3. 6 is as high as $\sim 10^{16}$ cm^{-3}, while that for nickel and copper is $\sim 10^{15}$ cm^{-3}. Thus, for the experiments of Section 3.2.2, rather high concentrations were used so as to be able to detect the metals using SIMS and TXRF and even then, metal concentrations could only be clearly measured in the porous silicon layer.

The most sensitive methods for probing the bulk contamination level of silicon are electrical techniques such as deep level transient spectroscopy (DLTS), surface photo-voltage (SPV) and other minority carrier lifetime measurement techniques such as microwave-detected photoconductance decay (μ-PCD) and simulation-assisted photoluminescence (sim-PL), both of which can be applied to epitaxial p/p$^+$ structures (as discussed further in Chapter 5). In this section, the impact of metal contamination on the quality of a epitaxial layer with an underlying porous silicon gettering layer is assessed directly by measuring the minority carrier lifetime mainly using μ-PCD and also sim-PL. Both techniques, in relation to measurements on epitaxial p/p$^+$ structures, are explained in detail in Chapter 5.2.1.

Samples were prepared as described in Section 3.1 (see Figure 3. 1). For the work of this section, the samples had a porous silicon of 400 nm thickness and ~28% porosity. Epitaxial layers with a boron doping concentration of $\sim 10^{16}$ cm^{-3} and thicknesses of 25, 30, 40 and 50 μm on top of a 2 μm p$^+$ silicon (boron doping concentration of 10^{19} cm^{-3}) BSF were grown. Only iron and nickel contamination of two different concentrations were used to deliberately contaminate the samples. The surface concentrations were 10^{12} cm^{-2} and 10^{13} cm^{-2} on the rear surface which should result in a bulk contamination level of $\sim 10^{13}$ cm^{-3} and 10^{14} cm^{-3}, respectively, if the metal impurities on the surface distributed uniformly throughout the silicon without significant evaporation losses. Minority carrier lifetime measurements were done before and after metal contamination and drive-in i.e. after step 3 and after step 7 in Figure 3. 1, respectively.

3.3.1 Minority carrier lifetime studies of iron gettering

An effective lifetime map obtained from a μ-PCD measurement of an uncontaminated epilayer sample is shown in Figure 3. 7 (a). The square-like pattern in the middle of the wafer corresponds to the area with an embedded porous silicon layer. The effective lifetime in this area is lower because the embedded porous silicon exacerbates the interface recombination at the interface between the epitaxial layer and the p$^+$ substrate compared to the peripheral area where there is no porous silicon present at the interface. This is studied in detail in Chapter 5 and 6, where it is concluded that despite the different effective lifetime

in the two areas due to the different effective interface recombination velocities, the bulk lifetimes in the two areas are comparable.

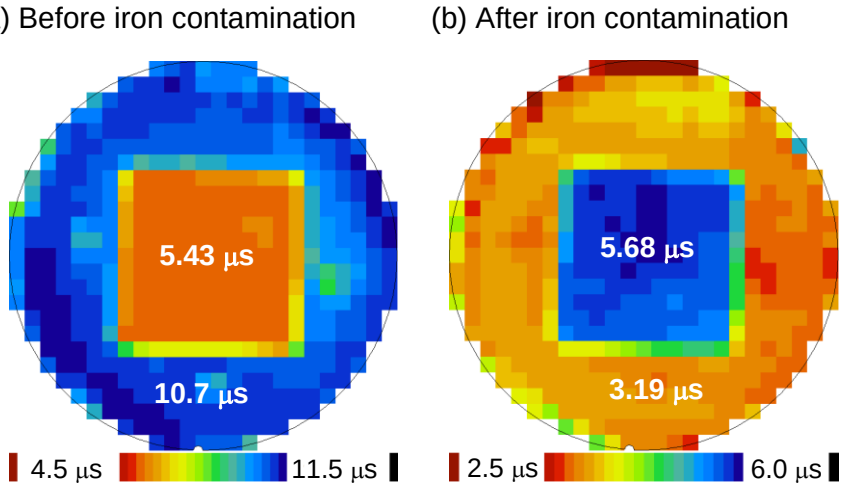

Figure 3. 7 Effective lifetime maps obtained from µ-PCD measurements on a 50 µm thick p-type (boron doping concentration of 10^{16} cm^{-3}) epitaxial layer shielded by a 2 µm thick p^+ silicon (boron doping concentration of 10^{19} cm^{-3}) BSF (a) before contamination, and (b) after rear-surface contamination, with a surface iron concentration of ~10^{12} cm^{-2}, and metal drive-in at a temperature of 1000 ^oC for 20 min, which would result in a bulk iron concentration of ~10^{13} cm^{-3} if uniformly distributed.

However, after contaminating the sample with a bulk iron concentration of ~10^{13} cm^{-3}, a remarkable reversal in the relative effective lifetime is observed. Now, the effective lifetime in the porous silicon area is higher than in the periphery, despite the higher interface recombination in the porous silicon area, as shown in Figure 3. 7 (b). After contamination, the epitaxial layer effective lifetime in the porous silicon area remains stable, while in the periphery, the effective lifetime drops. This clearly demonstrates the beneficial effect of iron gettering by porous silicon, which ensures that the epitaxial layer quality is more or less unperturbed despite a significant iron contamination level in the substrate.

One of the advantages of experiments based on iron is that the concentration of iron in the epitaxial layers can be determined via lifetime measurements by making use of the iron-boron pair dissociation reaction that can be activated by thermal or strong optical excitation of the sample. This idea was first proposed by Zoth and Bergholz in 1990 who determined iron concentration in silicon wafers by using the SPV method to measure the diffusion length before and after thermal dissociation of Fe-B pairs [9]. They claimed an iron detection sensitivity of 2-5×10^{11} cm^{-3}. This method has since been developed extensively to be used in conjunction with other minority carrier lifetime techniques such as quasi-steady state photoconductance (QSSPC) [10], [11], µ-PCD [12] and photoluminescence (PL) [13]–[15] at arbitrary doping and injection levels. The idea behind this method is explained in the coming paragraphs.

Iron in p-type silicon is a positively-charged interstitial impurity, Fe_i^+, which at room temperature is mobile at atomic length scales. In boron-doped silicon, the positively charged Fe_i^+ tends to pair with negatively-charged substitutional boron, B^-, to form immobile FeB pairs as follows

$$Fe_i^+ + B^- \leftrightarrow FeB \tag{3.1}$$

So, the principle behind this method involves the measurement of the minority carrier lifetime (or diffusion length) when the iron point defects in the sample exist predominantly as FeB pairs. Subsequently, a dissociation reaction is induced to convert (at least partially) the FeB pairs into Fe_i^+ interstitials. A second measurement of minority carrier lifetime (or diffusion length) is then made. The difference in the measured lifetimes is then proportional to the iron concentration as follows

$$[Fe] = C\left(\frac{1}{\tau_{diss}} - \frac{1}{\tau_{undiss}}\right) \tag{3.2}$$

where τ_{undiss} is the lifetime measured before dissociation and τ_{diss} is that after dissociation. C is a proportionality pre-factor that can be calculated based on SRH statistics.

The minority carrier lifetime in an iron-contaminated silicon sample depends on whether the iron exists as Fe_i^+ or FeB. This is because the SRH recombination parameters of the Fe_i^+ defect and the FeB defect are very different as was already indicated in Table 2.5 in Chapter 2, Section 2.1.2. Extensive work done by various researchers to ascertain the SRH parameters of both interstitial iron and iron-boron pairs is summarised in Table 3. 2.

For the Fe_i^+ defect, there is very good agreement about the hole capture cross-section of $\sim 7.0 \times 10^{-17}$ cm^2. For the electron capture cross-section of Fe_i^+, there is quite some uncertainty with Rein *et al.* reporting a value of 3.6×10^{-15} cm^2 that is about an order of magnitude smaller than the value of 4×10^{-14} cm^2 reported by Istratov *et al.* (which was supposed to have been taken from [9]). On the other hand, recently Paudyal *at al.* reported a value of 7.5×10^{-15} cm^2 which is in between the other two values. Yet, there remains some uncertainty as to the correct electron capture cross-section, which has also been discussed by Macdonald *et al.* in [16]. For the FeB defect too, there is uncertainty regarding both the electron and hole capture cross-sections. Researchers often tend to use their own values where available such that it fits their data well.

The SRH lifetimes due to the Fe_i^+ and FeB defects can be calculated based on the values given in Table 3. 2, and using the SRH lifetime equation (2.2) introduced in Chapter 2, Section 2.1.2. This has been done for the Fe_i^+ defect based on the carrier capture cross-section values from Istratov *et al.* [20] as well as Paudyal *et al.* [22], and for the FeB defect based on Macdonald *et al.* [16] and Paudyal *et al.* [22]. Plots resulting from such calculations, for an iron concentration of 10^{13} cm^{-3}, are shown in Figure 3. 8. As expected, the FeB defect has a weaker injection-level dependence compared to the Fe_i^+ defect.

Table 3. 2 The dominant defect energy level in the band gap of silicon and the corresponding carrier capture cross-sections for the interstitial iron defect (Fe_i^+) and the iron-boron pair defect (FeB), as reported in literature.

	E_t [eV]	σ_n [cm²]	σ_p [cm²]	k_σ	Reference
Fe_i^+	$E_V + 0.37$ $E_V + 0.39$	⋯	3.1×10^{-17}	⋯	Wunstel *et al.* (1982) [17]
	$E_V + 0.42$ $E_V + 0.52$	⋯	1.5×10^{-16}	⋯	Indusekhar *et al.* (1986) [18]
	$E_V + 0.37$	⋯	8.8×10^{-17}	⋯	Brotherton *et al.* (1985) [19]
	⋯	5×10^{-14}	⋯	⋯	Zoth *et al.* (1990) [9]
	$E_V + 0.38$	4×10^{-14}	6.9×10^{-17}	51	Istratov *et al.* (1999) [20]
	$E_V + 0.394$	3.6×10^{-15}	7.0×10^{-17}		Rein *et al.* (2005) [21]
	⋯	7.5×10^{-15}	6.6×10^{-17}	113	Paudyal *et al.* (2009) [22]
FeB	$E_C - 0.3$	2.5×10^{-15}	3×10^{-14}	0.08	Walz *et al.* (1996) [23]
	$E_C - 0.23$	3×10^{-14}	2×10^{-15}	15	Macdonald *et al.* (2001) [24]
	$E_C - 0.26$	1.4×10^{-14}	1.1×10^{-15}	13	Birkholz *et al.* (2005) [10]
	$E_C - 0.26$	2.5×10^{-15}	5.5×10^{-15}	0.45	Rein *et al.* (2005) [21]
	$E_C - 0.26$	5×10^{-15}	3×10^{-15}	1.7	MacDonald *et al.* (2006) [16]
	⋯	3.3×10^{-15}	1.4×10^{-15}	2.34	Paudyal *et al.* (2009) [22]

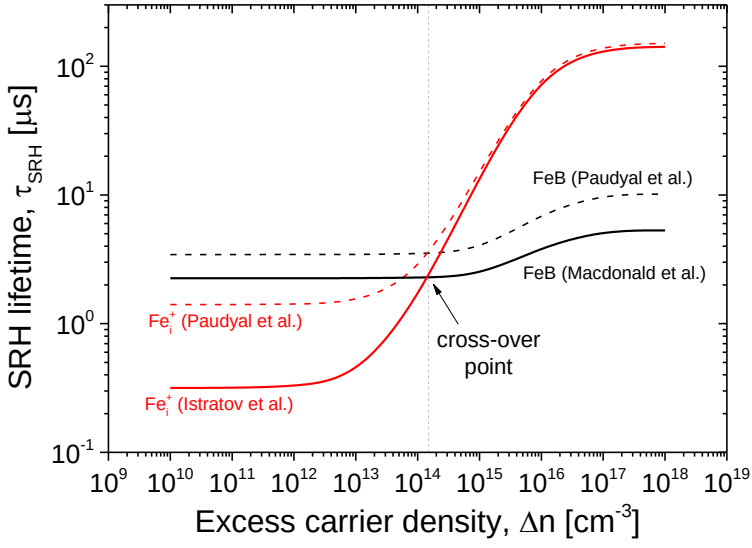

Figure 3. 8 The injection level-dependent SRH lifetime, calculated based on eqn. (2.2) (see Chapter 2) and the SRH recombination parameters of the Fe_i^+ and FeB defects as reported in [16], [20], [22], *for an iron concentration of 10^{13} cm^{-3}. In the calculation, it is assumed that iron only exists in one of the two forms.*

In general, for the same iron concentration, the SRH lifetime of an iron-contaminated sample will depend on the relative proportion of iron that exists as FeB pairs as opposed to Fe_i^+ interstitials. At one particular injection level, known as the cross-over point as indicated in Figure 3. 8, the SRH lifetime is invariant and independent of the form in which the iron point defects exist.

In Figure 3. 8, we can observe that there is a big difference in the SRH lifetimes of the Fe_i^+ defect below the cross-over point, while there is a good match in the high injection region. Thus, the differences in the SRH lifetimes of the Fe_i^+ defect is not critical for μ-PCD measurements which are done at high injection levels, but becomes important for injection levels close to or below the cross-over point.

One of the methods that is used to arrive at the carrier capture cross sections is the cross-over point method [16]. The carrier capture cross-section values are chosen such that the experimental data for the cross-over point is fitted well. In Figure 3. 8, we can see that the same cross-over point is obtained by choosing the carrier capture cross-section values of Istratov *et al.* and Macdonald *et al.* or by only using those of Paudyal *et al.* In fact, a similar observation is made with the capture cross-section values of Rein *et al.* as well (not shown in Figure 3. 8). Although any one of these sets of capture cross-section values can be used, we will use the capture cross-sections of Fe_i^+ from Istratov *et al.* [20] and those of FeB from Macdonald *et al.* [16], particularly because these values fit the cross-over point observed in the experiments of this thesis as well as the iron concentration data reasonably well.

Not only are the carrier capture cross-sections different, but the symmetry factor, k_σ, is also drastically different for the two defects, with the Fe_i^+ defect having a highly asymmetrical capture cross-section ($k_\sigma = 51$) compared to the FeB defect ($k_\sigma = 1.7$) [22]. This would imply a stronger injection level dependence of the SRH lifetime for the Fe_i^+ defect compared to the FeB defect.

The equilibrium constant of the reversible point defect reaction (3.1) was empirically found to be [25]

$$\frac{[\mathrm{FeB}]}{[\mathrm{Fe}_i^+][\mathrm{B}^-]} = 10^{-23}\exp\left(\frac{0.65}{k_B T}\right) \tag{3.3}$$

Therefore, for an epitaxial layer with a boron doping concentration, $N_{epi}(=[\mathrm{B}^-])$, of 10^{16} cm^{-3} at room temperature, 99.986% of iron point defects will exist as FeB pairs. These FeB pairs can be dissociated by heating up the sample to 200-300 ^oC [9] or by using strong illumination such as white light with an intensity of 0.1 Wcm^{-2} for 5 min [11].

Optical dissociation is preferable because it leads to 99% dissociation for the above illumination conditions [11] and since this happens at approximately room temperature, the re-association time of the Fe_i^+ interstitials to form FeB pairs is much longer than at high temperature. The characteristic time for re-pairing, τ_{pair}, is given by [9]

$$\tau_{pair} = 4.3 \times 10^5 \frac{T}{[\mathrm{B}^-]}\exp\left(\frac{0.68}{k_B T}\right) \tag{3.4}$$

which means for the epitaxial layers with a boron doping concentration of 10^{16} cm^{-3}, the $\tau_{assoc} = 49$ min at room temperature compared to only a few seconds at

200 °C. Typically, measurements in this thesis are done with 1 min of the optical dissociation for single point measurements and within 10 min for mapping measurements.

Thus, before dissociation, we can assume that almost all iron point defects exist as FeB pairs, while after strong optical dissociation, all iron point defects exist as Fe_i^+ interstitials within the time frame of the measurement.

Hence, the minority carrier lifetime of an iron-contaminated sample before dissociation, τ_{undiss} can be expressed as

$$\frac{1}{\tau_{undiss}} = \frac{1}{\tau_{\mathrm{FeB}}} + \frac{1}{\tau_{other}} \tag{3.5}$$

After dissociation, the minority carrier lifetime, τ_{diss}, can be expressed as

$$\frac{1}{\tau_{diss}} = \frac{1}{\tau_{\mathrm{Fe}_i^+}} + \frac{1}{\tau_{other}} \tag{3.6}$$

Here τ_{FeB} and $\tau_{\mathrm{Fe}_i^+}$ are the SRH lifetimes given by eqn. (2.2) presented in Chapter 2. τ_{other} includes all other components of the effective lifetime such as surface lifetime, Auger lifetime and SRH lifetime due to other defects. In the experiments of this thesis, it can be reasonably assumed that τ_{other} does not change during the dissociation. Thus, in taking the difference of the reciprocal of effective lifetimes in eqn. (3.2), this term cancels out. Thus, if the pre-factor C is known, then the concentration of iron in the sample can be evaluated.

The pre-factor, C, can be calculated by substituting eqns. (3.5) and (3.6) into eqn. (3.2) and using the SRH lifetime eqn. (2.2) for τ_{FeB} and $\tau_{\mathrm{Fe}_i^+}$, i.e.

$$\frac{1}{C} = \frac{1}{[\mathrm{Fe}]}\left(\frac{1}{\tau_{\mathrm{Fe}_i^+}} - \frac{1}{\tau_{\mathrm{FeB}}}\right) \tag{3.7}$$

where

$$\frac{1}{[\mathrm{Fe}]\tau_i} = \frac{N_{epi} + \Delta n}{\frac{1}{c_n^i}\left(N_{epi} + p_1^i + \Delta n\right) + \frac{1}{c_p^i}\left(n_0 + n_1^i + \Delta n\right)} \tag{3.8}$$

with

$$c_n^i = \sigma_n^i v_{th} \quad \text{and} \quad c_p^i = \sigma_p^i v_{th} \tag{3.9}$$

The superscripts "i" refer to either "Fe_i^+" or "FeB". c_n and c_p are the electron and hole capture coefficients, respectively. The other symbols have their usual meanings. The SRH parameters are given in Table 3. 2 and the doping density is usually well-controlled during epitaxy and is known. With this, the pre-factor C is plotted as a function of injection level in Figure 3. 9. Since during a μ-PCD measurement, the carrier density continuously decays, it is only possible to specify an effective average injection level, as mentioned in Chapter 5. This value should be between 5×10^{16} and 5×10^{17} cm^{-3}. In this range, C varies between -4.75×10^{13} and -5.00×10^{13} μs cm^{-3}. Thus, an average C value of -4.88×10^{13} μs cm^{-3} is used for the calculations.

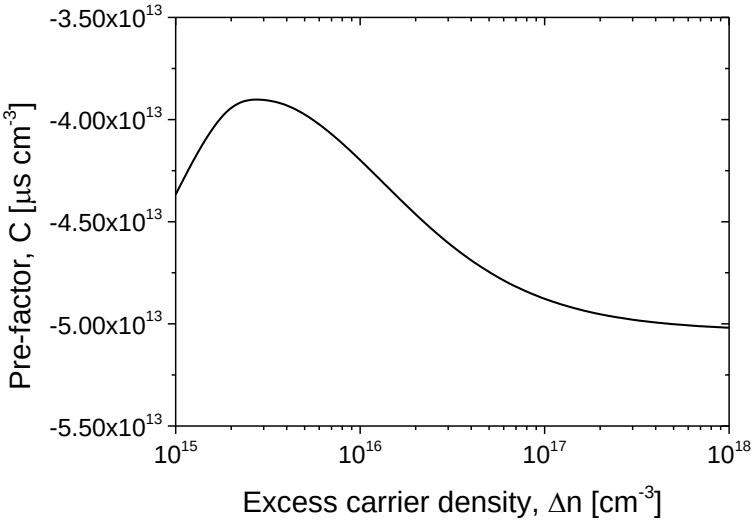

Figure 3. 9 Pre-factor C as function of injection level, calculated based on eqn. (3.7).

Two representative positions, one inside and one outside the porous silicon area, were picked from the lifetime maps shown in Figure 3. 7, and repeated measurements were done on the same spot. The measured lifetime is then plotted against the measurement time in Figure 3. 10, for both positions that are inside and outside the porous silicon area. Each point in the plot represents an average of 1024 measurements.

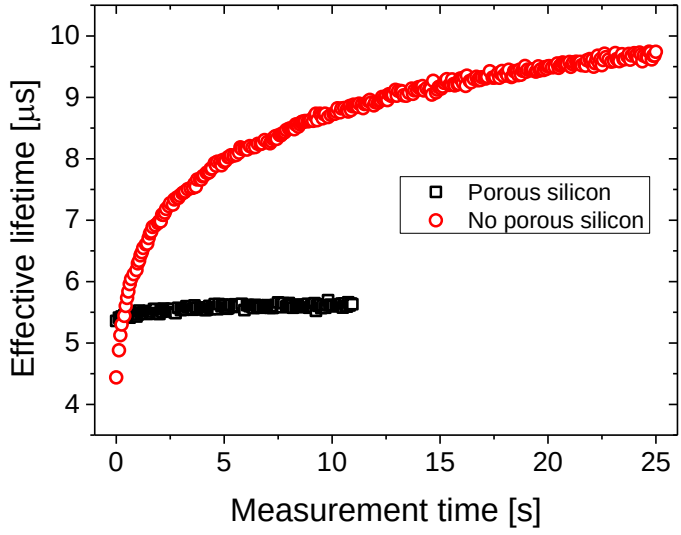

Figure 3. 10 Effective lifetimes obtained using µ-PCD measurements at two representative locations, one inside the porous silicon area and the other outside the porous silicon area, for a 50 µm thick p-type epitaxial p/p+ sample, with a target bulk iron contamination of 10^{13} cm^{-3}. The horizontal axis represents the progression of the repeated measurements.

A clear increase in the lifetime is observed with repeated measurements, at the end of which the lifetime appears to saturate at a higher value. The difference between the final lifetime and the initial lifetime is almost negligible in the porous silicon area while it is drastic in the area without porous silicon. This is because, with each successive measurement, a small fraction of iron that is present as FeB pairs would dissociate to form $\tau_{\mathrm{Fe}_i^+}$ interstitials, resulting in an increase of lifetime for next successive measurement. A smaller increase signifies a lower concentration of iron, according to eqn. (3.2). Thus, we can infer that the concentration of iron in the porous silicon area is almost negligible compared to the area without porous silicon.

In order to find the actual iron concentration, there should be almost no dissociation of the FeB pairs during the first measurement and there should be almost full dissociation during the second measurement. Since the illumination during the measurement itself perturbs the state of the sample, it is quite a challenge to measure the lifetime of a sample with undissociated FeB pairs. In order to get as close as possible to τ_{undiss}, low power measurements are done and the averaging is reduced from 1024 to 64. However, there is a trade-off because reducing the averaging increases the noise level of the measurements and thus the minimum detectable iron concentration. For the epitaxial p/p^+ samples and the measurement set-up used in this work, the average detection limit for iron concentration using the method described is estimated to be $\sim 7.5\times10^{11}$ cm^{-3}, which is more than four orders of magnitude lower than what is possible with SIMS (see for example Figure 3. 5).

Similar FeB pair dissociation experiments were performed on samples of different epitaxial layer thicknesses and for two different target bulk iron concentrations of 10^{13} cm^{-3} and 10^{14} cm^{-3}. After low power, low averaging measurements to obtain τ_{undiss}, the sample area was illuminated at high power until the lifetime saturates and a second lifetime measurement is made at the same power as the first measurement to obtain τ_{diss}. From such measurements, the iron concentration is calculated based on eqn. (3.2) and plotted in Figure 3. 11.

For the samples contaminated with a target bulk Fe concentration of 10^{13} cm^{-3}, it can be seen that the Fe concentration inside the porous silicon area is below the detection limit, while that outside the porous silicon area is well above the detection limit, except for 25 μm epitaxial layer, which is considered to be an anomalous result. When the contamination level is increased by an order of magnitude, similar observations can be made. The Fe concentration in the porous silicon area is close to or below the detection limit, while the concentration of Fe outside porous silicon attains a concentration well over 10^{13} cm^{-3}, but falls short of the target bulk iron contamination level of 10^{14} cm^{-3}. In all cases, the bulk Fe concentration is lower than the target concentrations due to evaporation losses and due to segregation gettering by the heavily-doped p^+ substrate, which is effective at lower temperatures [1], [26].

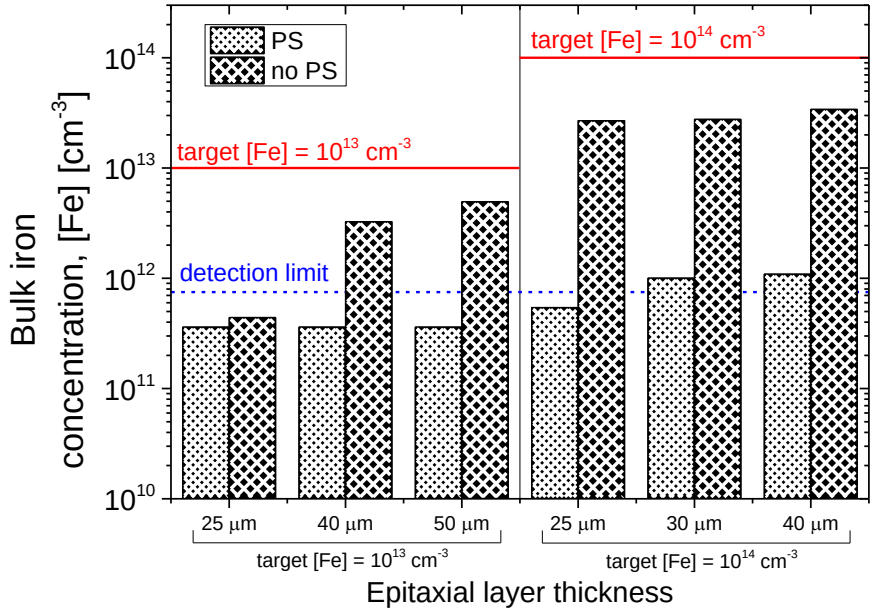

Figure 3. 11 Bulk metal concentration in the epitaxial layers of different thicknesses, obtained using the FeB pair dissociation method, both inside and outside the porous silicon area. Two sets of three samples were contaminated from the substrate rear surface to a target concentration of 10^{13} and 10^{14} cm^{-3}, respectively. The average detection limit and the target concentrations are also indicated.

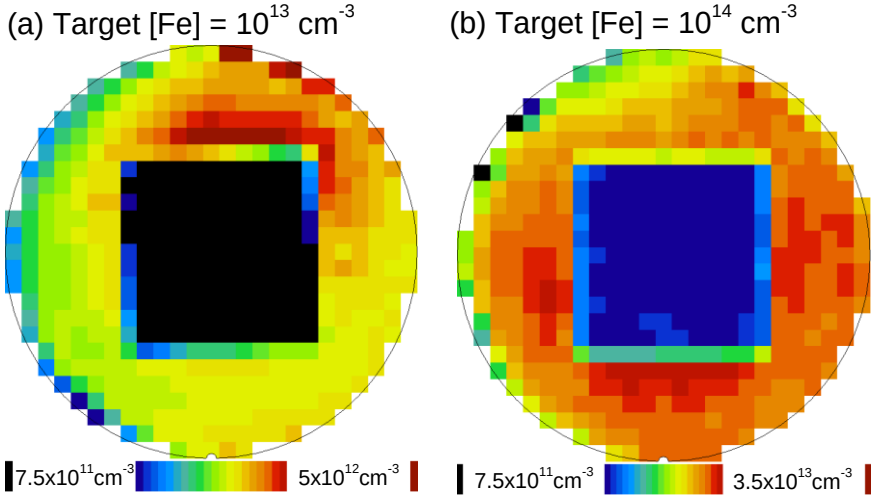

Figure 3. 12 Iron concentration distribution maps obtained using the FeB pair dissociation method using µ-PCD for (a) a 40 µm thick boron-doped epitaxial layer contaminated to a target iron concentration of 10^{13} cm^{-3}, and (b) a 25 µm thick boron-doped epitaxial layer contaminated to a target iron concentration of 10^{14} cm^{-3}.

Using μ-PCD, iron distribution maps across the wafer can be obtained by measuring the effective lifetime before and after FeB pair dissociation. For this, instead of local illumination, the entire wafer was illuminated by several (>20) flashes of white light to dissociate the FeB pairs in the whole sample at once and fast (small raster size of 4-8 mm) and low averaging (64) measurements were performed. The resulting τ_{diss} map together with the τ_{undiss} map such as the one in Figure 3. 7 can be used to obtain iron distribution maps, as shown in Figure 3. 12, where two iron maps are shown, one of each contamination level, of 10^{12} and 10^{13} cm^{-3}. Clearly, the iron concentration in the porous silicon area is much lower, as was already shown. In the sample with a target iron contamination level of 10^{12} cm^{-3}, the iron in the epitaxial layer on top of porous silicon is below the detection limit, whereas for the sample contaminated to a target concentration of 10^{13} cm^{-3}, it is close to the detection limits, agreeing well with the single point measurements. As for the area outside porous silicon, large concentrations of iron is detected.

This proves that by using porous silicon as a gettering layer, low concentrations of iron can be achieved in the epitaxial layer. Although there is a large uncertainty associated with iron concentration in the porous silicon area, since the values are close to the detection limit, if they are to be believed, then a large gettering efficiency of at least 10^2 can be estimated. This agrees well with what was concluded using the SIMS analysis of Figure 3. 5.

3.3.2 Minority carrier lifetime studies of nickel gettering

Nickel contamination experiments were also performed as mentioned at the beginning of this section. Epitaxial p/p^+ samples were prepared in the same way as the samples used in the iron gettering experiments. In these experiments, similar to iron gettering experiments, two metal bulk concentrations were used: 10^{13} and 10^{14} cm^{-3}.

Unlike Fe gettering experiments, the actual Ni concentrations cannot be estimated from lifetime measurements, since nickel does not interact with boron. Thus, in order to evaluate the impact of nickel on the bulk of the epitaxial layer in the presence / absence of porous silicon, efforts were made to estimate the bulk lifetime of epitaxial layers (τ_{epi}) by measuring the effective lifetime (τ_{eff}) on epitaxial layers of different thicknesses (d_{epi}), as described more in detail in Chapter 5, Section 5.2.1.3.

A linear fit of the simple equation, $1/\tau_{eff} = 1/\tau_{bulk} + S_{tot}/d_{epi}$ in a plot of $1/\tau_{eff}$ versus $1/d_{epi}$ would yield the bulk lifetime from the reciprocal of the $1/\tau_{eff}$ -axis intercept. S_{tot} is the sum of the effective surface and interface recombination velocities. For uncontaminated samples, sim-PL (described in Chapter 5 and 6) was used to evaluate the bulk lifetime. Although sim-PL is a low injection lifetime technique, for nickel-contaminated samples, this is not an issue since the symmetry factor, k_σ of nickel is 0.7 which is close to 1, which should result in a weak injection level dependence of the lifetime. Epitaxial layer bulk lifetimes evaluated in this way before contamination, and after contamination with nickel are summarised in Table 3. 3.

For a target bulk nickel concentration of 10^{13} cm^{-3}, the bulk lifetime of the epitaxial layer on top of porous silicon remains approximately the same (~100 μs),

indicating that the epitaxial layer on top of porous silicon is relatively contamination-free. However, the bulk lifetime of the epitaxial layer outside the porous silicon area is significantly reduced (~15 µs). On the other hand, for heavy contamination with a target bulk nickel concentration of 10^{14} cm^{-3}, lifetimes of epilayers in both areas are drastically reduced. The values in Table 3. 3 for this case are indicated in parenthesis because these are the averages of the effective lifetimes across epitaxial layer samples of different thicknesses. This was done because the effective lifetime did not vary with thickness.

Table 3. 3 Epitaxial layer bulk lifetimes extracted using sim-PL and µ-PCD in epitaxial p/p⁺ samples before and after contamination with nickel. Two target bulk nickel concentrations were used, namely, 10^{13} and 10^{14} cm^{-3}.

	Before contamination	[Ni] ≈ 10^{13} cm^{-3}	[Ni] ≈ 10^{14} cm^{-3}
Area with embedded porous silicon	100-125 µs	99.5 µs	(2.2 µs)
Ares without embedded porous silicon	100-120 µs	14.5 µs	(3.0 µs)

These results contradict with what was predicted as the tolerable nickel concentration to achieve 20 µs bulk lifetime in an epitaxial layer (see Figure 2.6 in Chapter 2). This indicates that nickel impurities that exist in the epitaxial layers probably do not exist as nickel point defects, but possibly as nickel silicide platelets in the bulk or are simply segregated to the front surface or both.

The first scenario implies that at high concentrations of nickel, the porous silicon trap sites could become saturated, with the excess nickel impurities remaining in the epitaxial layer. If these impurities are quenched as nickel silicide platelets, the bulk recombination will be far more enhanced compared to when nickel exists as point defects because small nickel silicide platelets form deep band-like states in the band gap of silicon with an electron capture cross of $\sim 5\times10^{-14}$ cm^2 in n-type silicon [27] and as high as 10^{-12}-10^{-10} cm^2 [28] in p-type silicon, which are much higher than the capture cross-section of $\sim 5.6\times10^{-17}$ cm^2 for nickel point defects in silicon (see also Figure 2.1 or Figure 2.6).

In the second case, it has been observed experimentally that nickel not only segregates to porous silicon but also to the front surface. In comparison to the porous silicon surfaces which are not in direct contact with the active epitaxial layer bulk (separated by a BSF), nickel segregation to the front surface would severely reduce the effective lifetime of the epitaxial layers by severely increasing the front surface recombination and to an extent the bulk recombination in the near surface region.

Thus, it can be concluded that a porous silicon stack with a thickness of 400 nm and a porosity of 28% is very effective up to a bulk nickel concentration of $\sim 10^{13}$ cm^{-3}. Increasing the trap density of porous silicon could potentially increase the gettering capacity for nickel and other metals.

3.4 Chapter summary

- A procedure for intentional metal contamination and gettering in epitaxial p/p^+ structures, starting from clean substrates, is presented. The metal contamination is done spin-coating known concentrations of a metal solution on the back surface of the wafer, followed by high temperature annealing for metal drive-in (Figure 3. 1). On the same wafer, there are areas with and without embedded porous silicon.
- The front surface metal concentrations of such contaminated and gettered samples were analysed by total reflection X-ray fluorescence (TXRF).
- Even for high concentrations of metal contamination ($\sim 10^{16}$ cm^{-3}), there is little or no metal impurities detected on the surface of the epitaxial layer in the porous silicon area, whereas the surface metal concentration outside the porous silicon area is orders of magnitude higher than the detection limits, for all tested metal impurities (iron, nickel and copper).
- The in-depth bulk metal concentration of such contaminated and gettering samples is analysed by secondary ion mass spectroscopy (SIMS).
- Large accumulation of iron, nickel and copper is observed in the porous silicon layer, while the metal concentration in the surrounding silicon is below detection limits.
- Large gettering ratios of $>10^3$ for copper and nickel and $>10^2$ for iron are estimated, which agrees well with modelling results of Chapter 2.
- Slower cooling rate leads to better gettering characteristics.
- Minority carrier lifetime measurements are performed on epitaxial p/p^+ structures before and after contamination with iron and nickel using microwave photoconductance decay (μ-PCD) and simulation-assisted photoluminescence (sim-PL).
- For uncontaminated epitaxial p/p^+ structures, the effective lifetime is lower inside the porous silicon area due to a higher interface recombination. After contamination with [Fe] of $\sim 10^{13}$ cm^{-3}, the epitaxial layer lifetime outside the porous silicon area becomes lower than that inside the porous silicon area, where the lifetime remains stable despite the contamination. For an [Fe] of $\sim 10^{14}$ cm^{-3}, the lifetime in both areas are reduced but the reduction is minimal in the porous silicon area.
- Optical dissociation of iron-boron pairs together with lifetime measurements before and after dissociation is used to estimate the iron concentration in the epitaxial layers. For both contamination levels, the iron concentration in the epitaxial layers on top of porous silicon is below or close to the detection limits, while that outside the porous silicon area is very high.
- A large gettering ratio of $\sim 10^2$ is determined, agreeing well with the SIMS results of this chapter and the modeling results of Chapter 2.
- In nickel gettering experiments, for a [Ni] of $\sim 10^{13}$ cm^{-3}, the epitaxial layer bulk lifetime remained stable in the porous silicon area at ~100 μs, while it

dropped to ~15 μs outside the porous silicon area. For the higher [Ni] of ~10^{14} cm^{-3}, lifetime in both areas are significantly reduced. Thus, porous silicon gettering of nickel for the studied porous silicon stack is effective up to a [Ni] of ~10^{13} cm^{-3}.

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Chapter 4
Transition Metal Gettering by Porous Silicon: Enhancing the Gettering Efficiency

In this chapter, the possibility of enhancing the gettering efficiency of porous silicon by tuning its properties, and in particular the mean void size in the porous silicon layer is systematically explored both theoretically and experimentally.

In Chapter 3, in the discussion surrounding the SIMS depth profiles of Figure 3.5, it was pointed out that the large metal accumulation in the porous silicon consists of two sub-peaks, one of them being higher than the other. This higher peak corresponds to the lower porosity layer with a distribution of smaller voids, while the lower peak coincides with the higher porosity layer with a distribution of larger voids. This suggests that by reducing the void size, the gettering efficiency could be increased.

4.1 Theoretical insight into the void size dependence of metal gettering

4.1.1 Thermodynamics of metal binding to curved surfaces

Metal segregation to the void surfaces is driven by an overall reduction of the total free energy of the system. As discussed by Schiettekatte *et al.* [1], from thermodynamics of curved surfaces, the contribution of the surface curvature to the chemical potential, β, of a spherical surface such as a void with radius, r, is associated with the surface energy, γ, as follows

$$\beta = \Omega \frac{2\gamma}{r} \tag{4.1}$$

where Ω is the molecular volume of silicon. When a system containing such a void is in equilibrium with metal impurities in the bulk of silicon, it follows readily that a curved surface is preferable for metal segregation over a flat surface. From

(4.1), it is also clear that the smaller voids with a larger surface curvature will be more preferential gettering sites than larger voids.

4.1.2 *Ab initio* modeling of metal binding in the V29 void

In Chapter 2, Section 2.2.2, we discussed *ab initio* calculations based on density functional theory (DFT), from which the binding energy of Cu and Fe atoms to void surface trap sites were determined. Two different void sizes were tested, namely V29 and V35, where the number indicates the number of silicon lattice sites constituting the void. The results of the binding energies obtained from the larger V35 void were summarised in Table 2.8.

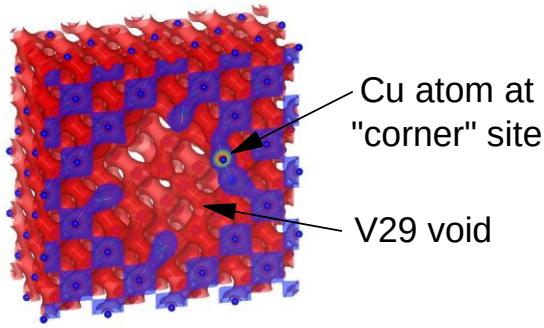

Figure 4. 1 Electron density plot of a void structure, containing the V29 void, obtained from a converged DFT simulation, showing a copper atom bound to a surface trap site.

Here, the results of the simulations performed with the V29 void structure is presented to gain atomistic insight into the void size dependence of gettering. The electron density plot resulting from a converged simulation for the binding of a copper atom at a surface site of the V29 void structure is shown in Figure 4. 1. This particular binding resulted in a very high binding energy of ~4.12 eV, which is much higher than the highest binding energies reported for the V35 void structure in Table 2.8. Besides this, another simulation also yielded a large binding energy of ~3.65 eV. Despite exhaustively simulating all non-equivalent trap sites on the V35 void surface, such high binding energies could not be obtained.

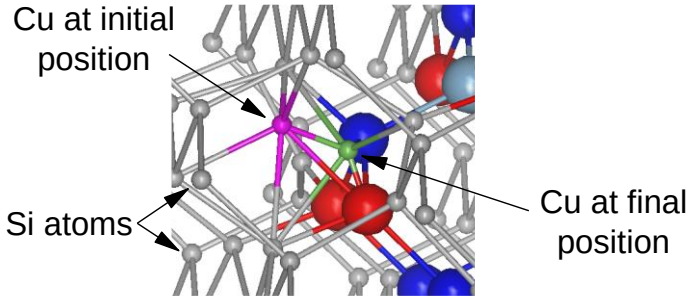

Figure 4. 2 Atomic structure of a converged DFT simulation showing the initial and final positions of a copper atom at a surface site of the V29 void (which is depicted by the large spheres, red and blue, which are actually the silicon lattice sites). Silicon atoms are grey in colour. The lines between the atoms do not always represent bonds.

In order to understand the origin of these large binding energies, the atomic structure of the converged simulation corresponding to Figure 4. 1 was investigated, as shown in Figure 4. 2. The pink-coloured atom in Figure 4. 2 indicates the copper atom at an tetrahedral interstitial site (T-site) at the beginning of the simulation. During the simulation, due to minimisation of total energy, the copper atom relaxes to the final equilibrium position indicated by the green-coloured atom in Figure 4. 2. In this final position, the copper atom is coordinated with 3 silicon atoms with an inter-atomic distance of ~2.4-2.5 Å in a tri-bonding configuration, thus stabilising three DBs. The location of this trap site is one of the corners of the truncated octahedron forming V29. Even for simulations with the V35 void structure, the most energetically favourable binding sites were at corners or edges of the void structure where the density of dangling bonds is probably higher in comparison to the facets. However, in the smaller V29 void, due to the strong curvature and the resulting atomic geometries, there exist corner sites where the copper atom was able to coordinate more strongly than in corner sites of the V35 void, thus resulting in a higher binding energy.

Both V29 and V35 voids are very small compared to realistically-sized voids. In much larger voids, the proportion of facet binding sites would increase in comparison to corner and edge binding sites. This can already be seen by comparing the void structures V29 and V35 as shown in Figure 2.11 (a) and (b) respectively. The empty lattice sites of the voids are colour-coded according the number of dangling bonds (DBs) that result from the removal of a silicon atom from each void lattice site when creating the void. There is a greater DB density on the surface of the V29 void in comparison to that of the V35 void. Since one of the mechanisms that lower the total energy during gettering is dangling bond passivation, one can expect a higher average binding energy for metal binding in smaller voids compared to large ones.

From this exercise, it can be expected that due to the greater proportion of “corner” and “edge” binding sites in smaller voids, the average binding energy would be higher in smaller voids, making them more preferable for metal binding.

4.2 Experimental studies of void size dependence of metal gettering

The void size distribution can be controlled by means of the thickness and porosity of the porous silicon layer during the electrochemical etching process. The thickness is varied by the etch duration, while the porosity is varied by the applied current density or the electrolyte concentration. Thicker layers and higher porosity result in pore size distributions that are shifted towards larger pore sizes.

4.2.1 Gettering efficiency enhancement by void size reduction

All samples in this work were prepared in a similar manner to those discussed in Chapter 3, Section 3.1, as schematically shown in Figure 3.1, except when the differences are specified.

In the first set of experiments, the porous silicon thickness was varied between 160 nm and 1430 nm. The porosity of the porous silicon was kept constant at ~28% by fixing the current density. The wafers were contaminated with a mixed solution of Cu, Ni and Fe to a surface metal concentration $\sim 10^{15}$ cm^{-2} for each metal and annealed at 1000 ^{o}C for 15 min. The samples were then analysed by SIMS depth profiling to obtain the metal concentrations in porous silicon. Cross-sectional scanning electron microscopy (SEM) was used to obtain the sizes of the porous silicon voids.

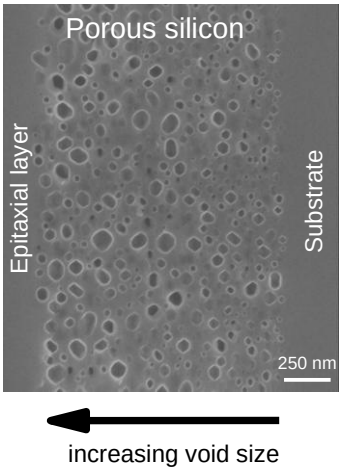

Figure 4. 3 A cross-sectional SEM image of the 1430 nm-thick embedded porous silicon layer showing the void size distribution in depth, right being deeper and closer to the substrate (which is 730 μm thick).

The SEM image of the thickest porous silicon sample investigated (1430 nm) is shown in Figure 4. 3. A clear trend is discernible whereby the void size distribution changes from larger voids near the epitaxial layer side to increasingly smaller voids towards the substrate side. This can be explained using the classical porous silicon sintering theory proposed by Labunov *et al.* using vacancy diffusion processes [2], which has been explained in detail in Chapter 7, Section 7.1.2.1.

Central to this theory are three key concepts which are revisited here in order for the subsequent explanation to make sense. Firstly, porous silicon reorganisation is driven by vacancy supersaturation and vacancy gradients between the pores/voids and their surroundings. Secondly, the vacancy concentration around a pore/void is inversely proportional to its radius. Thirdly, there exists a critical void radius, below which voids shrink and dissolve, and this radius is inversely proportional to the vacancy supersaturation [3]. i.e. the higher the vacancy supersaturation, the smaller the critical void radius.

Based on this, the void size distribution of Figure 4. 3 can be explained. During reorganization, the wafer surface acts as a vacancy sink since the vacancy concentration there tends to its thermodynamic equilibrium value, which is very small compared to the supersaturated vacancy concentration between the voids/pores. This results in a drop in the vacancy concentration towards the surface, which transports vacancies away from the near-surface side of the porous

layer to the wafer surface, thus reducing the vacancy supersaturation in that part of the layer. This in turn causes the critical void radius to increase there, resulting in the shrinkage of small voids, leading to a predominance of large voids over small ones. This effect then propagates deeper into the porous silicon, since a vacancy concentration gradient exists between the near-surface part of the porous silicon (having larger voids) and the deeper areas of the porous silicon, resulting in a gradual shrinkage of small pores closer to the substrate. This results in a distribution of void sizes from larger voids near the surface to smaller ones deeper in the porous silicon. This is equivalent to the Ostwald ripening phenomenon in solid solutions [4]–[6] which leads to an overall increase in void size throughout the layer.

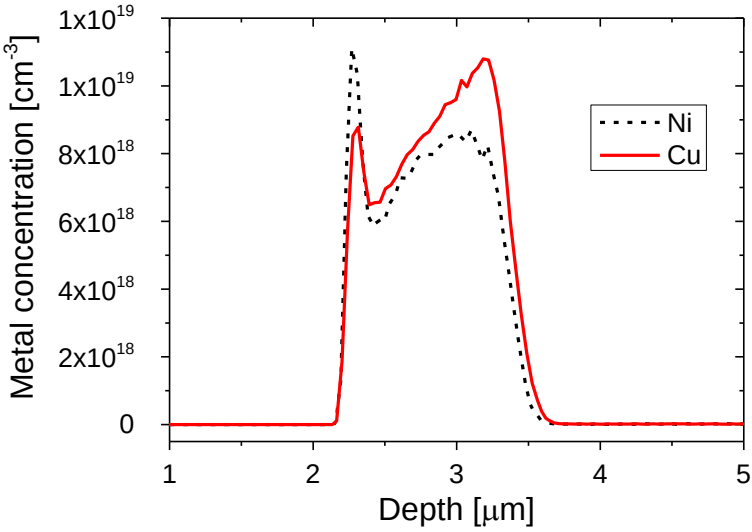

Figure 4. 4 Metal concentration profiles in depth obtained by SIMS depth profiling in an epilayer/porous silicon/substrate stack that was surface-contaminated with a mixed metal solution containing nickel and copper to a surface concentration of ~10^{15} cm^{-2} and annealed at 1000 ^{o}C for 15 min. The porous silicon layer has the microstructure shown in Figure 4. 3.

SIMS depth profiling measurements performed on the sample of Figure 4. 3 are presented in Figure 4. 4 for Cu and Ni. A clear peak is observed as before at the depths where porous silicon exists. However, in order to elucidate the fine features of this peak, the measurements are plotted in linear scale. Two distinct features are noticeable.

Firstly, there is a sharp peak of high metal concentration at the interface between the porous silicon and the epilayer. One possible explanation for this is that the metal atoms are being gettered by interfacial defects such as misfit dislocations which occur during epitaxial growth if the porous silicon surface is imperfect (such as incompletely closed voids and roughness).

Secondly, beyond this narrow peak, the metal concentration in the porous silicon monotonically increases in depth. This corresponds to the trend seen in the SEM image whereby the void size distribution gradually tends towards smaller voids deeper in the porous silicon. This clearly indicates that smaller voids are

more effective in gettering Cu and Ni than voids of larger radii. Note that the area factor was found to be negligible.

To further illustrate this void size dependence of gettering, samples with different porous silicon void sizes were analysed with SEM and SIMS. These samples did not show the above-mentioned trend in void size distribution in depth. A median void size was then calculated based on lognormal fits to the void size distributions [3] obtained from several SEM images, as illustrated in Figure 4. 5.

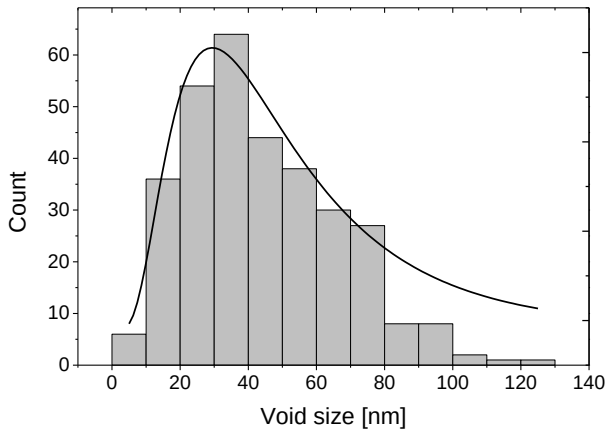

Figure 4. 5 Distribution of void sizes in a 400 nm thick porous silicon layer, fitted using the lognormal distribution to find the median void size.

From SIMS depth profiles of Cu, Ni and Fe on each of the samples, the corresponding gettering ratios, η_{gett}, (defined as the metal concentration in porous silicon over that in the substrate) were calculated. These gettering ratios as a function of the void diameter is plotted in Figure 4. 6 (a), which shows a strong enhancement in the gettering efficiency of porous silicon as the median void size is reduced. As before, the area factor accounting for the differences in the internal surface area between the samples is negligible. Significantly, the porous silicon layer with a median void size of 27.2 nm is > 13 times more efficient at gettering Cu and Ni compared to that with a median void size of 39.8 nm. Likewise, it is also > 7 times more efficient at gettering iron.

Comparing the biggest and smallest void sizes in this study (27.2 nm and 39.8 nm), the effect of additional curvature of the smaller void on the binding energy can be estimated using eqn. (2.21) by considering that the porous silicon systems are in equilibrium with the substrate in these samples, i.e.

$$\Delta E_B = k_B T \ln \frac{\eta_{gett,1}}{\eta_{gett,2}} \tag{4.2}$$

where ΔE_B refers to the enhancement in binding energy and the subscripts "1" and "2" refers to the porous silicon layers with a median void size of 27.2 nm and 39.8 nm respectively. A binding energy enhancement of ~288 meV for copper, ~285 meV for nickel and ~216 meV for iron results. These are considerably higher than 130 meV reported by Schiettekatte *et al.* for gold gettering for a larger void size range of 24 nm. This is probably because Ni, Cu and Fe are much smaller than

gold and hence can accommodate better at the "corner" sites described in Section 4.1.2.

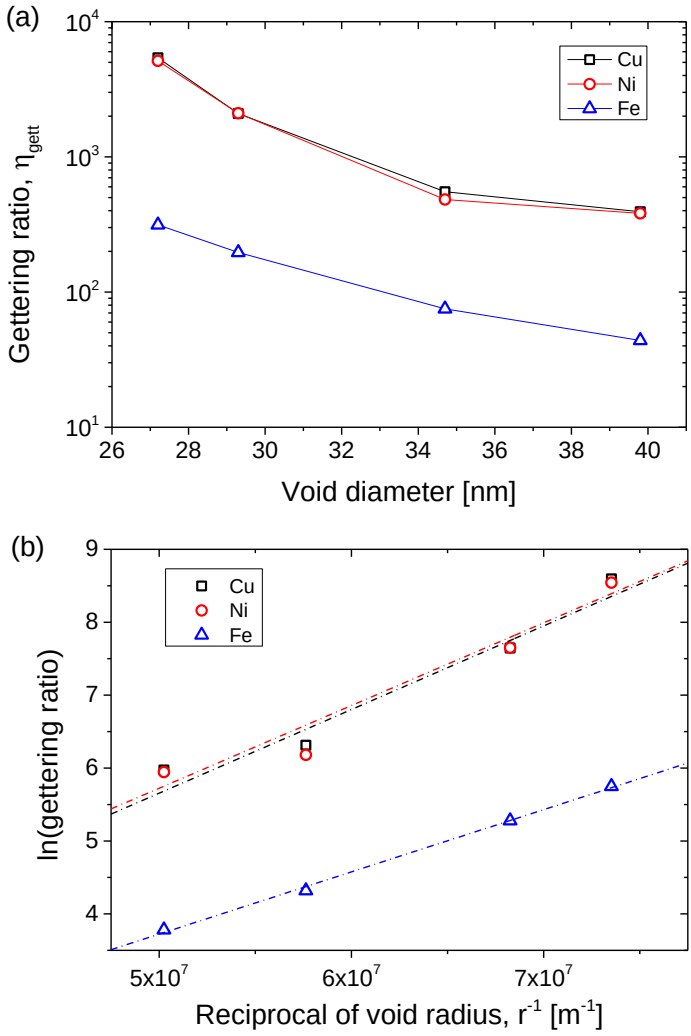

Figure 4. 6 (a) Plot of the gettering ratio, η_{gett}, defined as the ratio between the trapped metal concentration in porous silicon to that in the substrate, versus the median void diameter. (b) The same data points re-plotted showing the natural logarithm of the gettering ratio as a function of reciprocal void radius.

To correlate this binding energy enhancement with the theoretical insight gained in Section 4.1, the natural logarithm of the gettering ratio is plotted as a function of the reciprocal of the void radius, r, as shown in Figure 4. 6 (b). Good linear fits are obtained which indicate that the binding energy has a component with a $1/r$ –dependence. At first sight, this agrees well with the $1/r$ –dependence in eqn. (4.1). Realistic voids that have attained equilibrium shapes consist of facetted surfaces bound predominantly by low energy {111} and {100} surfaces

connected by {311} and {110} surfaces [3], [7]. The gradients of the fit lines of Figure 4. 6 (b) were compared with $\Omega\frac{2\gamma}{k_BT}$ values calculated for each of the facets based on surface energy values for different facets taken from [7], which showed that the values obtained from Figure 4. 6 (b) were ~26-41 times higher than the calculated equivalents. This clearly indicates that the increase in binding energy is not due to metal atom binding to void facets but rather to the trap sites in the corners and edges of a void, agreeing well with the *ab initio* simulations presented in Section 4.1.2 and Section 2.2.2 where significantly larger binding energies were obtained at "corner" sites.

Thus, the $1/r$ –dependence of Figure 4. 6 (b) cannot be explained using classical thermodynamics surrounding eqn. (4.1). Schiettekatte *et al.* [1] also found binding energy enhancement for gold gettering that was 2-4 times higher than what was expected from simple surface energy arguments. This was attributed to surface reconstruction effects. Based on our atomistic understanding of metal gettering, the $1/r$ –dependence can be understood using simple geometric scaling arguments for the density of binding sites. When comparing porous silicon layers with approximately similar internal surface area, as the average void size in the porous silicon is reduced, the density of edges and corner sites scales inversely in proportion to r. As a result, in porous silicon with smaller voids, the density of higher energy binding sites would be greater. This explains the $1/r$ –dependence observed in Figure 4. 6 (b).

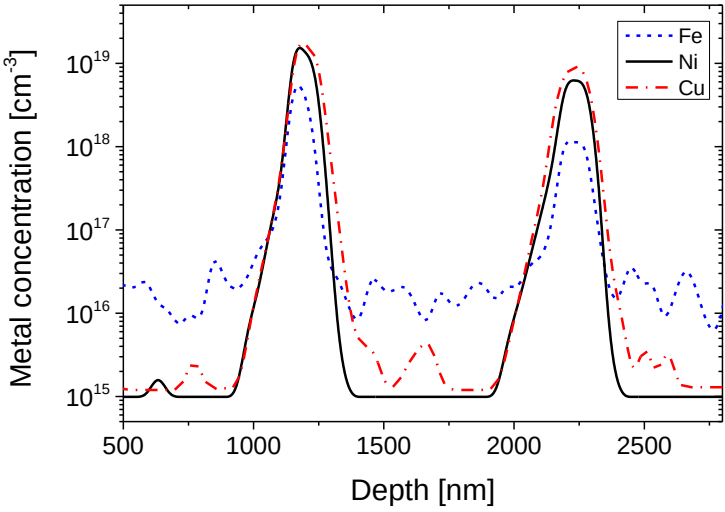

Figure 4. 7 Metal concentration profiles in depth obtained by SIMS depth profiling in an epilayer/porous silicon/substrate stack that was surface-contaminated with a mixed metal solution containing iron, nickel and copper to a surface concentration of ~10^{15} cm^{-2} and annealed at 1000 ^{o}C for 15 min. The porous silicon stack consists of two porous silicon layers separated by a 0.8 µm thick epitaxial silicon. The layer closer to the wafer surface has a porosity of 28% while that deeper in the substrate has a higher porosity of 41%.

In another experiment, an epitaxial layer sample was prepared such that two porous silicon layers were etched in the same wafer, separated by 0.8 µm-thick epitaxial silicon. This was done in two steps, whereby the second porous silicon

layer is etched on the epilayer that is grown after the high temperature reorganisation of the first porous silicon layer. The porous silicon layer closer to the surface had a porosity of ~28% and the porous silicon layer deeper in the substrate had a porosity of ~41%. The higher porosity layer has a larger median void size compared to the lower porosity layer. The contamination and processing steps used were similar to the previous experiment of this section.

Figure 4. 7 shows the metal concentration distribution in such a sample for all three metals. Two separated peaks corresponding to the two porous silicon layers can be observed, as expected. The metal concentration peaks for all metals are significantly higher in the lower porosity layer (the one on the left in Figure 4. 7) compared to the higher porosity layer. The fact that the metal contamination is introduced on the substrate side of the sample proves that this observation is not a result of a diffusion barrier effect of the first porous silicon layer.

Thus, in the face of all the experimental evidences given so far, porous silicon with smaller voids appears to getter more efficiently than one with larger voids.

4.2.2 Improvement of epitaxial layer lifetime by enhanced gettering

If the efficiency of porous silicon gettering is increased by reducing the median void size in the layer, this should result in a lower concentration of metals and thus higher minority carrier lifetime in the epitaxial layer. In order to check this, intentional contamination experiments were performed. In contrast to the processing sequence followed in the previous experiments, a different approach was taken which allows injection level-dependent lifetime measurements to be made. This is illustrated in Figure 4. 8.

Double-side mirror polished, 750 μm-thick Czochralski (Cz)-grown silicon wafers with a boron doping concentration of 3×10^{15} cm^{-3} were used. The idea is to contaminate, getter and measure the minority carrier lifetime in the bulk of this wafer. Porous silicon gettering of epitaxial layers is a proximity gettering technique (20-50 μm) but the wafer is an order of magnitude thicker than typical epitaxial layers. Since the focus of this work is on the gettering of proximal silicon, the 750 μm thick wafers was thinned down by silicon etching using 5% tetramethyl ammonium hydroxide (TMAH) by volume in water at 80 ^{o}C for more than 12 h to attain a final thickness of ~210-220 μm.

Subsequently, epitaxial deposition of a 3 μm-thick p^+ silicon epitaxial layer with a boron doping concentration of 10^{19} cm^{-3} (step 1 in Figure 4. 8) is carried out twice, once on each surface of the wafer. This step is needed in order to etch a layer of porous silicon. While the p^+ silicon on one surface is needed for the formation of mesoporous porous silicon, the p^+ silicon on the other surface is needed to form an ohmic contact with the chuck that supplies the current for the etching, since the wafer itself forms the anode during the electrochemical etching process. Following epitaxy, an 800 nm thick porous silicon is etched electrochemically (step 2 in Figure 4. 8), as described in previous sections, with two different current densities, namely, 1.38 and 5.40 $mAcm^{-2}$ which results in porous silicon of two different porosities, which were not characterised in these experiments.

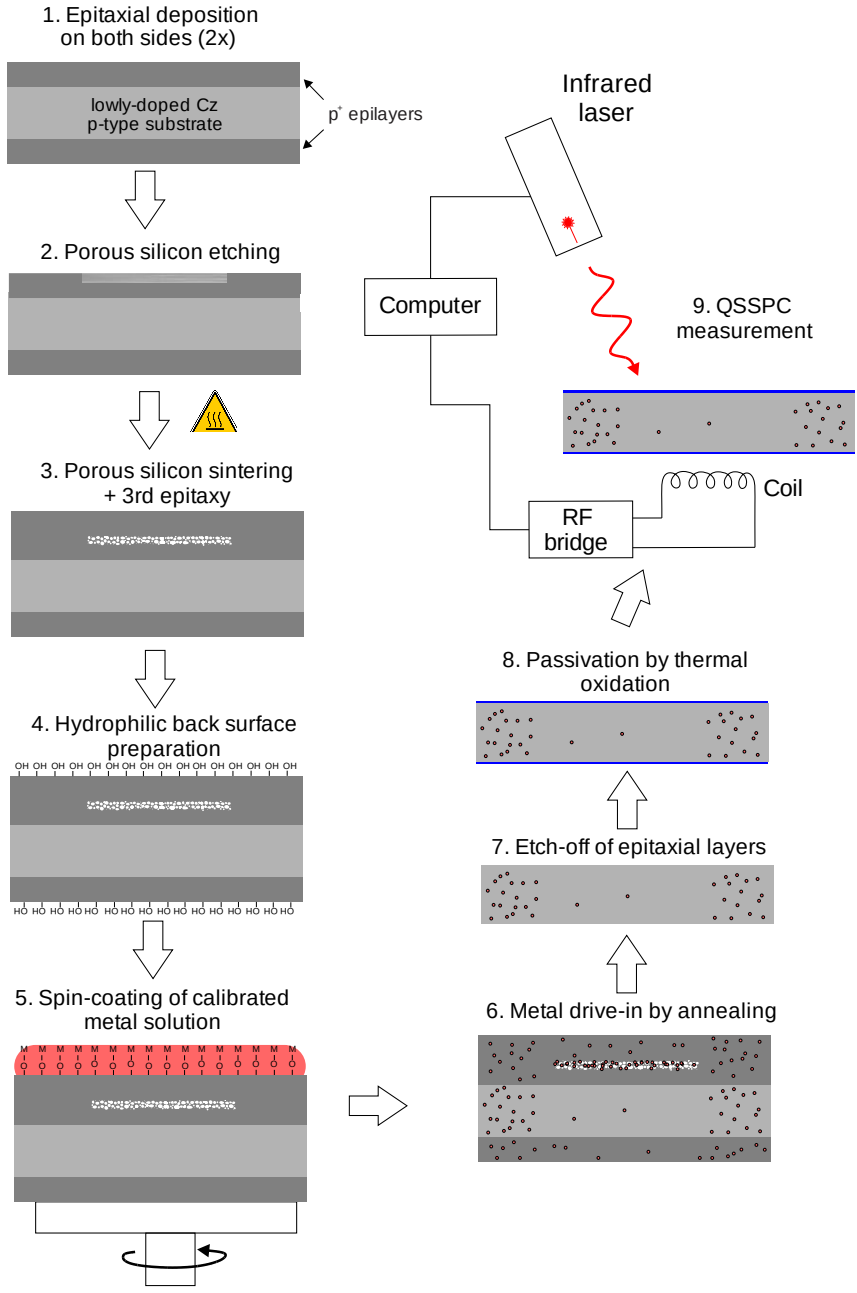

Figure 4. 8 Process flow used for intentional metal contamination and gettering experiments, where the substrate itself is gettered by porous silicon which is etched on an epitaxial layer i.e. a reversed configuration to the WE-epicell structure. Note that the proportions and dimensions are not to scale.

This is followed by sintering of porous silicon at 1130 ^{o}C for 10 min and the deposition of a 2 µm-thick p^+ silicon with a boron concentration of 10^{19} cm^{-3} on top of the annealed porous silicon (step 3 in Figure 4. 8), which has also be described in earlier sections. This thin epitaxial layer represents the "substrate" of the WE-epicell and the lowly-doped, high quality substrate itself represents the "epitaxial layer" of the WE-epicell, i.e. a reversed configuration.

This is then followed by processes which are similar to those discussed with Figure 3.1, where the wafer surfaces are made hydrophilic by treating them in an ammonium hydroxide-hydrogen peroxide mixture (APM) (step 4 in Figure 4. 8). This is then followed by the contamination of the wafer surface closest to the porous silicon by spin coating of known concentration of metals (step 5 in Figure 4. 8). The metals tested in these experiments are iron and copper. Two different surface iron concentrations (10^{12} and 10^{13} cm^{-2}) and one surface copper concentration (10^{13} cm^{-2}) were tested. Metal drive-in at 1000 ^{o}C for 20 min (step 6 in Figure 4. 8) is then performed.

Subsequently, the epitaxial layers on both surfaces are etched off using a chemical polishing solution (step 7 in Figure 4. 8), consisting of acetic acid (CH_3COOH), 50% hydrofluoric acid (HF) and 69% nitric acid (HNO_3) i.e. CH_3COOH : HF : HNO_3 = 1:1:8. This is an aggressive mixture which etches off silicon at a rapid rate of 0.05 µm s^{-1}. The etching is performed for about 3 min to remove close to 30 µm from each surface. In order to remove any metal contaminants from the surface which can be driven in during the next step, the wafers were dipped in diluted 5% hydrochloric acid in water for 5 min, which would remove most of the metal impurities on the surfaces. This is followed by a dip in dilute 2% HF for 2 min to make the surfaces hydrophobic.

Next, the wafers are passivated by a ~140 nm thick silicon oxide layer grown by thermal oxidation performed at 1050 ^{o}C (step 8 in Figure 4. 8). The minority carrier lifetime of the samples are then measured by quasi-steady state photoconductance (QSSPC) [8]. This is described in further detail in Chapter 5. For the iron gettering samples, iron-boron pair dissociation method is used to determine the iron concentration, as described in Chapter 3, Section 3.3.1.

In the first experiment, two samples, one of each porosity, prepared as described above were contaminated with a surface iron concentration of 10^{13} cm^{-2}. The median void size estimated using SEM measurements for the lower porosity layer is 36.7 and the higher porosity layer is 40.0 nm. In the following discussion, they are simply referred to as "small voids" and "large voids" respectively.

Minority carrier lifetime measurements were performed on these samples before and after dissociation of iron-boron pairs. A white light with an intensity of 0.1 Wcm^{-2} for 5 min was used to dissociate the iron-boron pairs in the sample. The resulting injection-dependent effective lifetimes obtained using QSSPC before and after dissociation are shown in Figure 4. 9. It is observed that the effective lifetime of the sample which was gettered by small voids is much larger than that which was gettered by large voids, both before dissociation and after dissociation. This suggests that the iron concentration in the sample that is gettered by porous silicon with smaller voids is lower than one gettered by porous silicon with larger voids.

Iron-boron dissociation experiments were performed to calculate the actual iron concentration in the samples. After iron-boron pair dissociation, the effective lifetime increases at injection levels higher than the cross-over point, while it decreases below the cross-over point. The cross-over point occurs at an injection level of 7×10^{13} cm^{-3}. This agrees very well with what is predicted using the Fe_i^+ defect carrier capture cross-sections from Istratov *et al.* [9] and the FeB defect carrier capture cross-sections from Macdonald *et al.* [10], for the doping concentration of the substrate which is 3×10^{15} cm^{-3}. It should be noted that other combinations of carrier capture cross-sections described in Chapter 3, Section 3.3.1 also fits the data regarding the position of the cross-over. Thus, it seems reasonable to use the chosen carrier capture cross-sections from literature.

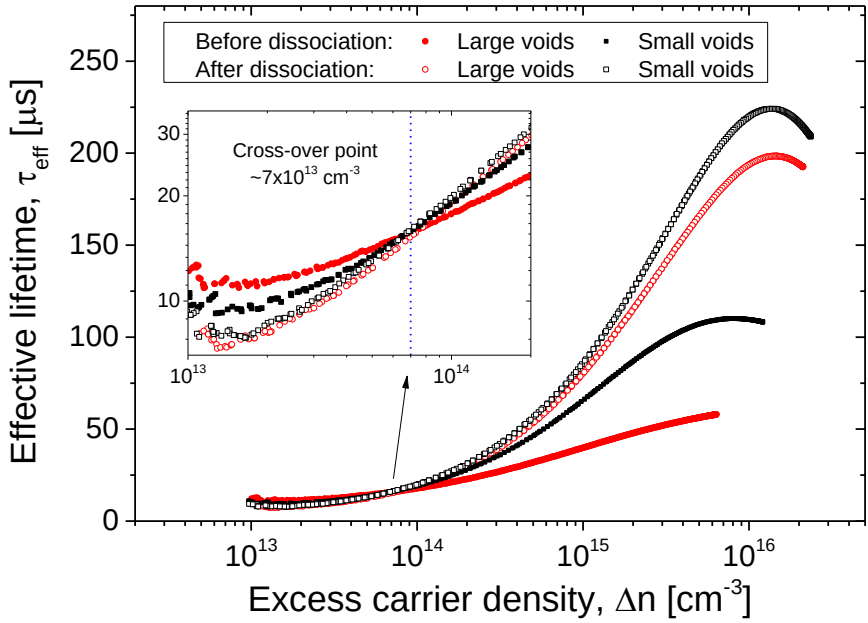

Figure 4. 9 Injection level-dependent effective lifetimes obtained using QSSPC before and after iron-boron dissociation, for two samples gettered by two different porous silicon layers with different void sizes (called "large" and "small"). The samples were prepared as described in Figure 4. 8 and contaminated with iron to a surface iron concentration of 10^{12} cm^{-2}. Inset shows the cross-over point in a log-log scale.

In order to calculate the iron concentration from the difference in the lifetimes before and after dissociation, injection levels greater than 10^{15} cm^{-3} were used. At lower injection levels, there is much greater uncertainty regarding the carrier capture cross-sections, as explained in Chapter 3, Section 3.3.1. The iron concentrations in both samples were calculated at 5 different injection levels based on eqns. (3.2) and (3.7) given in Chapter 3, Section 3.3.1 and plotted in Figure 4. 10. Remarkably, the iron concentration calculated at different injection level using different lifetime values and different pre-factor *C* are relatively similar, which demonstrates the robustness of this method.

The iron concentration in the sample gettered by porous silicon with larger voids is about 3 times higher than that in the sample gettered by smaller voids,

demonstrating that porous silicon with smaller voids have higher gettering efficiency. Assuming that all iron impurities on the surface after spin-coating is driven into the bulk of the silicon, the gettering ratio can be estimated to $\sim 10^2$ for the porous silicon with large voids and 3 times more for that with small voids. The order of magnitude seems to match results from the previous sections very well.

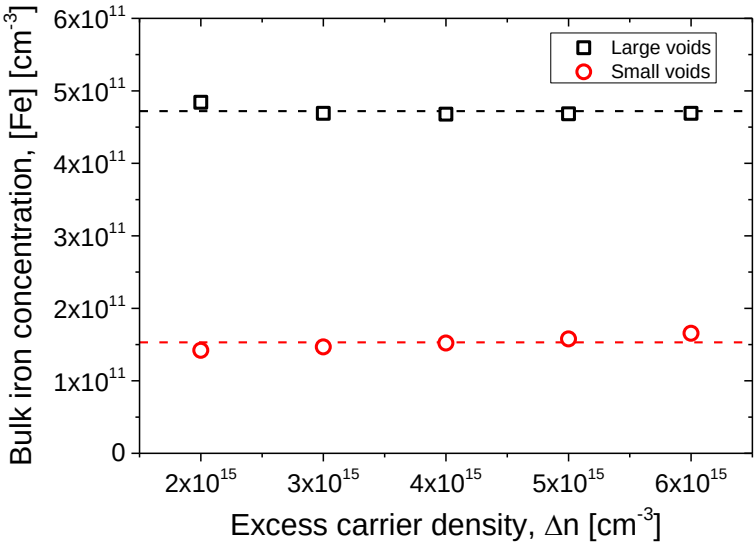

Figure 4. 10 Bulk iron concentration estimated using the iron-boron pair dissociation method for different excess carrier densities, in two samples gettered by porous silicon with large and small voids, respectively. The dotted line indicates the average iron concentration in each sample.

The same experiments were performed with a higher iron concentration of 10^{14} cm^{-2}. From the resulting injection level-dependent lifetime curves, the same observations can be made. The lifetimes are higher at all measurement injection levels in the sample gettered by the porous silicon with smaller voids compared to that gettered by the porous silicon with larger voids. However, due to the much higher contamination level in these samples, effective lifetimes could not be measured at injection levels greater than 10^{15} cm^{-3} and 6×10^{14} cm^{-3} for the sample gettered by small and large voids respectively. Under these conditions, extracting the iron concentration using the iron-boron dissociation method is not very reliable. Nevertheless, it was still tried out. The average iron concentrations are 3.5×10^{12} cm^{-3} and 2.2×10^{12} cm^{-3}, for the samples gettered by large and small voids respectively, which makes the porous silicon with smaller voids about 1.6 times more efficient than the one with larger voids.

In addition to iron gettering experiments, copper contamination and gettering was also performed in exactly the same way as described for iron earlier in this section. The surface copper concentration used was 10^{13} cm^{-2}. The resulting injection level-dependent effective lifetimes for two similar samples with two different voids sizes are shown in Figure 4. 11. The effective lifetimes at high injection in the sample gettered by porous silicon with smaller voids is clearly much better than that gettered by porous silicon with larger voids.

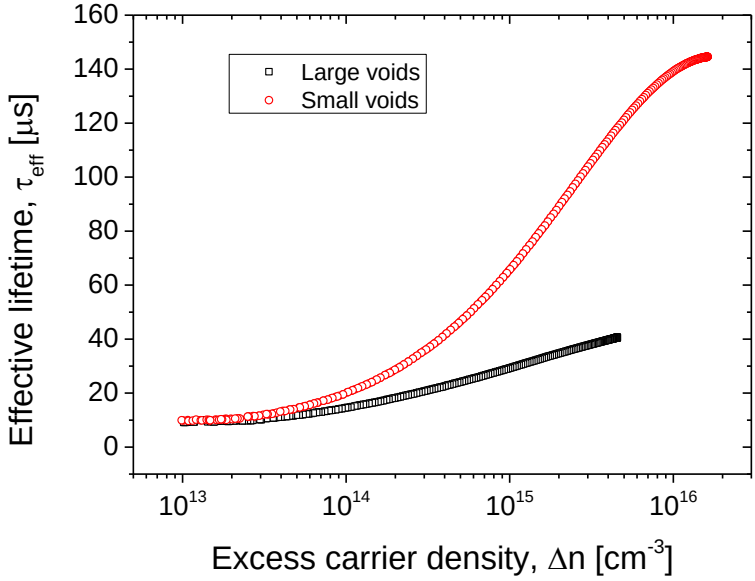

Figure 4. 11 Injection level-dependent effective lifetimes obtained using QSSPC, for two samples gettered by two different porous silicon layers with different void sizes (called "large" and "small"). The samples prepared as described in Figure 4. 8 and contaminated with copper to a surface copper concentration of 10^{13} cm^{-2}.

In conclusion, it has been proven that the gettering efficiency of porous silicon can be improved significantly by reducing void sizes in the porous silicon, by controlling the porosity and thickness of the porous silicon during etching.

4.3 Chapter summary

- Curvature thermodynamics indicates that metal segregation to curved surfaces is preferred to flat surfaces and the greater the curvature, the more energetically-favourable the segregation.
- *Ab initio* modeling using density functional theory (DFT) indicates that the most energetically favourable binding sites are those that exist at the corners and edges defining a facetted void. In particular, for the smaller V29 void structure, extremely large binding energy values, e.g. ~4.12 eV were obtained in corner binding sites, in contrast to larger V35 void structures.
- Analysis of a high binding energy site in the V29 void structure showed up to 3 dangling bonds stabilised by a single metal atom at a corner kink made possible by the strong curvature of the V29 void.
- Experimentally, an increase in the gettering efficiency was observed with a reduction in median void size in the porous silicon for all metals (Cu, Ni and Fe). In the investigated void size range (27.2 nm to 39.8 nm), the gettering efficiency is enhanced by more than >13 times for Cu and Ni and > 7 times

for Fe for the porous silicon with a median void size of 27.2 nm compared to that with a median void size of 39.8 nm.

- The corresponding binding energy enhancement was estimated to be ~288 meV for Cu, ~285 meV for Ni and ~216 meV for Fe. This enhancement is much stronger than that expected using curvature arguments of classical thermodynamics (eqn. (4.1)).
- For facetted voids that have attained equilibrium shapes, the binding sites at the corners and edges of the void play an important role in metal gettering. The larger average binding energy and the concomitant gettering efficiency in porous silicon with smaller voids is due to increase in the density of edge and corner binding sites which scales inversely with the void radius.
- Minority carrier lifetime measurements on iron- and copper- contaminated and gettered samples show that the sample gettered by a porous silicon layer with a smaller median void size was significantly higher than that gettered by a porous silicon layer with a larger median void size.
- Optical iron-boron pair dissociation combined with minority carrier lifetime measurements showed that the iron concentration in a sample gettered by porous silicon with a median void size of 36.7 nm had 3 times less iron than one that was gettered by porous silicon with a median void size of 40.0 nm.
- This proves that porous silicon gettering can be enhanced by a reduction in the median void size of the porous silicon layer.

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Chapter 5
Lifetime measurements in epitaxial layers: Theory and Modeling

In both wafer-equivalent epitaxial silicon solar cells (WE-epicells) and layer-transferred epitaxial silicon solar cells (LT-epicells), silicon epitaxial growth is performed on annealed porous silicon. Thus, the annealed porous silicon surface is the seed for the epitaxial process. Chapters 5-7 are devoted to understanding the potential of annealed porous silicon as a template for the epitaxial growth of high quality films. Minority carrier lifetime measurements in the epitaxial layers are used to assess the quality of the epitaxial layer. In this chapter, the theoretical framework and measurement methodology needed for understanding and interpreting lifetime measurements on epitaxial layers (both when attached to a p^+ substrate and when detached from it) are discussed.

5.1 Minority carrier lifetime measurements in epitaxial layers

Porous silicon is crucial as an embedded Bragg reflector and gettering layer in WE-epicells and as an enabler of the layer transfer process in LT-epicells. Therefore, it is by design rather than choice that epitaxial films have to be grown on porous silicon.

5.1.1 Influence of porous silicon on the effective lifetime of epitaxial layers

There are several ways in which porous silicon can influence the effective minority carrier lifetime in an epitaxial film. Firstly, prior to epitaxy, since the epitaxial growth starts on the annealed porous silicon surface, the morphological and topographical nature of this surface will significantly influence the epitaxial

growth process. Even though the sintering process leads to a closed surface, there is still a probability that there will be open voids and other defects on the porous silicon surface. In addition, as will be shown in later sections, the surface roughness of the growth surface depends strongly on the nature of the porous silicon. These imperfections could lead to crystal defects such as dislocations and stacking faults during epitaxial growth of silicon, which would reduce the quality of the epilayer. For instance, it has been observed that the etch pit density after a short defect etch of an epilayer deposited on top of porous silicon is ~1-2 orders of magnitude higher than that of an epilayer deposited on bare silicon [1]. Moreover, it was also observed that in some circumstances the open-circuit voltage (V_{OC}) of WE-epicells with porous silicon is about 20 mV lower than that of WE-epicells without porous silicon. However, this V_{OC} dependence is not systematic [2].

Secondly, during epitaxy, the intrinsically-present stress distribution in the porous silicon layer as a whole will evolve and can cause strain during epitaxial growth itself and/or during the cool-down and subsequent processing sequence. Unwanted high stresses can have a negative impact on the quality of the epitaxial film as will be shown in Chapter 7.

Thirdly, as discussed in Chapters 2-5, for WE-epicells fabricated on low-cost substrates, there is considerable amount of metal impurities in the parent substrate which can diffuse into the epitaxial film during high temperature processing, thereby reducing the epitaxial layer lifetime. It was shown that the presence of porous silicon ensured a higher lifetime is achieved in the epitaxial film due to its gettering properties. It is also known that high-quality Cz-grown, "clean", p^+ silicon is likely to contain more transition metal impurities than lowly-doped Cz silicon, since metal impurities prefer to segregate to highly-doped silicon, and also because of its relaxed specification criteria. Since the starting substrate for both cell concepts is p^+ silicon, the role of porous silicon in lowering the concentration of recombinative point defects in the epitaxial film through gettering might become important even when these cell concepts are employed on relatively clean substrates.

Finally, for the case of WE-epicells, since the epitaxial film remains attached to the p^+ silicon parent substrate in the final device, the intermediate porous silicon stack presents a highly recombinative interface between the epitaxial film and the substrate due to the fact that it consists of a large enclosed surface area that is unpassivated. While the front surface can be easily passivated, the highly-recombinative interface may only be shielded with the use of a back surface field (BSF), since the rear "surface" of the epitaxial layer cannot be accessed in this cell concept. The interface recombination is expected to reduce the effective lifetime of the minority carriers in the epitaxial film.

Thus, porous silicon can have an effect not only on the bulk lifetime of the epitaxial film but also, in the case of the WE-epicell, on the interface recombination velocity. So, it is also useful to decouple the measured effective lifetime into bulk and surface components where possible. Minority carrier lifetime studies were done on epitaxial films both when they are attached to the p^+ substrate and detached from it. The former is relevant not only in the concept of WE-epicells, but

also important in monitoring the epitaxial film quality at an early stage for the LT-epicells. Moreover, a comparison of the epitaxial layer lifetime before and after detachment would yield information on the effect of the detachment process on the quality of the epitaxial film.

5.1.2 Challenges for the measurement of lifetime in silicon epitaxial layers

Measuring carrier lifetime in epitaxial films both when attached to the p^+ substrate and when detached from it has several challenging practical constraints, as summarised in Table 5. 1. These constraints affect not only the methods applicable for measuring lifetime in epitaxial films but also the sample preparation itself.

For attached epilayers, one of the main constraints is the presence of the p^+ substrate, which will influence the lifetime measurement depending on the technique. For instance, the commonly-used quasi-steady state photoconductance (QSSPC) technique [3] cannot be used in this case because the highly-doped substrate saturates the detector. This limits the applicable lifetime measurement techniques to those that are sensitive to the first tens of microns of silicon and those that have provisions for both optical excitation and detection/measurement from the front side (front-front configuration). Techniques which can be used in a front-front configuration include those based on microwave reflectance measurement, namely microwave-detected photoconductance decay (μ-PCD) [4]–[6] and microwave phase shift (μW-PS) [7], as well as those based on photoluminescence detection, namely, simulation-assisted steady-state photoluminescence (sim-PL) [8], [9] and quasi-steady state photoluminescence (QSSPL) [10]–[12].

Table 5. 1 Practical constraints and the applicable methods for lifetime measurements in epitaxial films.

Epilayer type	Constraints	Applicable methods
Attached to p+ substrate (WE-epicell)	Heavily-doped substrate can influence measurement Epilayer/substrate interface recombination is high and unknown	μ-PCD, sim-PL, microwave phase shift (μW-PS)
Detached from p+ substrate (LT-epicell)	Free-standing epifoils are fragile for handling Reaction of silicone (used as glue for bonding epitaxial foils to glass) with wet etchants during subsequent processes could adversely affect the surface passivation and/or the adhesion of the epitaxial foil. Interaction of silicone with plasma during deposition of passivation layer could lead to poor surface passivation.	QSSPC, μ-PCD, PL, μW-PS, etc.

Next, the rear side of the epilayer is the interface between the epilayer and the substrate which is not accessible for passivation. Therefore, the interface recombination velocity could be rather high, especially when the only protection from the highly recombinative porous silicon surfaces is an epitaxially-grown back

surface field (BSF). This exasperates the difficulty of distinguishing the contribution of bulk recombination from surface recombination in the measured lifetime.

On the other hand, for epilayers that are detachable from the substrate by means of the high porosity detachment layer, most of the lifetime measurements techniques such as QSSPC, μ-PCD and PL can be used. However, the first challenge is in the handling of these very fragile 20-50 μm thick epitaxial foils. It is clear that there are no tools readily available for handling such thin epitaxial foils in a free-standing manner without significant yield loss through breakage. Thus, a lifetime measurement methodology is introduced in this work, whereby the epitaxial film, while still attached to the parent substrate, is bonded to a glass carrier using a transparent glue (e.g. silicones) and then detached from the parent silicon substrate. In this way, these fragile epifoils are mechanically supported by a robust carrier throughout the processing and measurement sequence.

However, by using this glass-bonded configuration, other complications arise due to the presence of silicone in the structure. Wet chemicals used to process glass-bonded epitaxial foils must not react aggressively with silicone so that the rear surface is amenable for good passivation and the epitaxial foil is not delaminated from the glass.

Finally, the silicones used to bond the epitaxial foils to glass can interact with the plasma during the deposition of the passivation layer, resulting in a degradation of the passivation, if nothing is done to prevent and minimise this interaction [13], [14]. Thus, in the lifetime measurements, a shielded configuration is used, whereby the silicon area is larger than the silicone area, such that there are no silicones exposed directly to the plasma during the deposition. Alternatively, or in addition, dielectric masking to mask exposed silicon areas or local modification of exposed silicone can also be done [15].

5.2 Lifetime measurements on epitaxial films attached to a heavily-doped parent substrate

5.2.1 Effective minority carrier lifetime in asymmetrically-passivated p/p^+ silicon structures

In evaluating the quality of an epitaxial layer grown on annealed porous silicon, we need an appropriate reference. For epitaxial layers attached to a p^+ silicon substrate, an appropriate reference is an epitaxial layer grown on pristine silicon. Thus, four different configurations are considered for lifetime measurements on attached epilayers, based on whether there is a porous silicon layer embedded at the interface between the epitaxial layer and substrate or not, and if that interface is shielded with a back-surface field (BSF) or not. For simplicity, minority carrier lifetime studies were only performed on p-type epilayers, corresponding to the base region of a WE-epicell, that are grown on p^+ silicon substrates i.e. a simple p/p^+ structure. The cross-section of such an epitaxial p/p^+ structure with an

embedded porous silicon layer shielded by an epitaxially-grown BSF is depicted schematically in Figure 5. 1. All relevant physical, material and optical parameters related to the substrate and the epitaxial film are also defined.

For the substrate, by virtue of its heavy doping, the substrate minority carrier bulk lifetime, τ_{sub}, is assumed to be intrinsically limited by Auger recombination [16]. The minority carrier diffusion length and diffusion coefficient in the substrate are denoted as L_{sub} and D_{sub}. The rear surface of the substrate is not passivated and the effective surface recombination velocity at that surface, denoted as S_{rear}, is taken to 10^4 or 10^5 cm/s [17], [18]. These parameters remain the same for all four cases.

For the epilayer, the minority carrier bulk lifetime, diffusion length and diffusion coefficients, denoted τ_{epi}, L_{epi} and D_{epi} respectively, can be expected to depend on whether the epitaxial layer is grown on pristine p⁺ silicon substrate or on top of reorganised porous silicon. This is because, as explained before, the epitaxial films for these two cases have different epitaxial growth templates (pristine silicon versus reorganised porous silicon) and experience different gettering (porous silicon gettering versus p⁺ silicon substrate gettering, if any). These cases are distinguished with the subscripts "no PS" and "PS" respectively. Table 5. 2 summarises the nomenclature used for the different configurations.

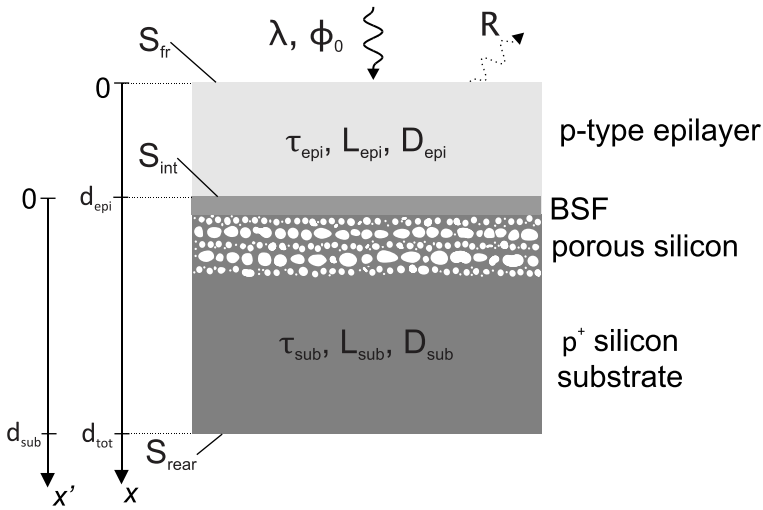

Figure 5. 1 Cross-section of the test samples used in the experiments, showing the most general case of a p-type epitaxial film (with a boron doping concentration of 10^{16} cm^{-3}) stacked on top of a p⁺ silicon substrate (with a typical boron doping concentration of 10^{19} cm^{-3}). A porous silicon layer is embedded in the substrate at the interface between the epitaxial layer and the substrate. An epitaxially-grown back surface field (BSF) of p⁺ silicon is also shown. Two depth axes have been defined, namely x and x', with the origins starting at the epilayer layer surface and the low-side of the high-low junction at the interface, respectively.

Similarly, the epitaxial layer / p⁺ silicon substrate interface is modelled by means of an effective surface recombination velocity, S_{int}, which will be exasperated by the presence of porous silicon, since it presents a highly

recombinative region at the interface. Thus, a similar distinction with subscripts "no PS" and "PS" is also made for S_{int}. In addition, the presence of a BSF will also modify the effective interface recombination velocity, since it provides a potential barrier to repel minority carriers away from the interface. This is distinguished with the subscript "BSF" in Table 5. 2 as $S_{int,no\ PS/BSF}$ and $S_{int,PS/BSF}$.

Table 5. 2 Definition of symbols for the epitaxial layer bulk lifetime and effective interface recombination velocity for four different configurations of p/p⁺ epitaxial structure depending on the presence/absence of the embedded porous silicon and back surface field (BSF).

	No porous silicon		Porous silicon	
No BSF	$\tau_{epi,no\ PS}$,	$S_{int,no\ PS}$	$\tau_{epi,PS}$,	$S_{int,PS}$
BSF	$\tau_{epi,no\ PS}$,	$S_{int,no\ PS/BSF}$	$\tau_{epi,PS}$,	$S_{int,PS/BSF}$

The effective interface recombination velocity is proportional to a recombination current density (J_{rec}^{int}) flowing through a virtual surface placed just in front of the low-side of the high-low junction (d_{epi}^{-}) [19]. This recombination current is due to the recombination at the interfacial defects as well as the leakage of excess carriers over the p/p⁺ low-high barrier. Thus, there are two components to this current density (or equivalently the surface recombination velocity), namely a current density due to recombination at the defects in the interface region ($J_{rec}^{defects}$ or $S_{defects}$) and a current density due to the leakage of minority charge carriers across the potential barrier into the substrate (J_{rec}^{BSF} or S_{BSF}), i.e.

$$J_{rec}^{int} = J_{rec}^{defects} + J_{rec}^{BSF} \quad \text{or} \quad S_{int} = S_{defects} + S_{BSF} \tag{5.1}$$

The effective interface recombination velocity at the low-side of a high-low junction has been derived by Godlewski *et al.* [20] and extended to include band gap narrowing (BGN) by Rohatgi *et al.* [21] as follows

$$S_{BSF} = \frac{D_{sub} N_{epi}}{L_{sub} N_{sub}} \mathrm{e}^{\left(\frac{\Delta E_{G,sub}}{k_B T}\right)} \frac{\frac{S_{rear} \cdot L_{sub}}{D_{sub}} + \tanh\frac{d_{sub}}{L_{sub}}}{1 + \frac{S_{rear} \cdot L_{sub}}{D_{sub}} \cdot \tanh\frac{d_{sub}}{L_{sub}}} \tag{5.2}$$

with

$$\Delta E_{G,sub}(N) = K_1 \ln\left(\frac{N_{sub}}{K_2}\right) \tag{5.3}$$

Band gap narrowing in the heavily-doped substrate, denoted as $\Delta E_{G,sub}$, is described by a simple logarithmic function as indicated in eqn. (5.3) for the purposes of modeling [22], [23]. The values of $K_1 = 14$ meV and $K_2 = 1.4 \times 10^{17}$ cm^{-3} (the doping concentration for the onset of BGN) have been adopted for the calculations and simulations in this thesis based on the work of Klaasen *et al.* [24]. Due to the effect of BGN [25], there is a minima between in the effective interface recombination velocity between the doping concentrations of 10^{18} and 10^{19} cm^{-3} as shown in Figure 5. 2.

For a mirror-polished starting substrate without an embedded porous silicon layer, one would expect negligible interfacial defects, and so $S_{int,no\ PS}$ and

$S_{int,no\ PS/BSF}$ would be approximately equal, since the main contribution to the interface recombination would then come from the drain of carriers over the high-low barrier.

The front surface of the epitaxial layer is passivated with aluminium oxide or silicon dioxide and the effective front surface recombination velocity is denoted as S_{fr}, which is conservatively assumed to be 10 cm/s throughout this work. The samples are illuminated from the front (epitaxial layer side) with monochromatic light of wavelength, λ and incident flux density, ϕ_0. The front surface reflectivity is denoted as R. Thus, there are 6 different parameters to be extracted, summarised in Table 5. 2, to understand the influence of porous silicon in terms of the lifetime characteristics of epilayers attached to a substrate.

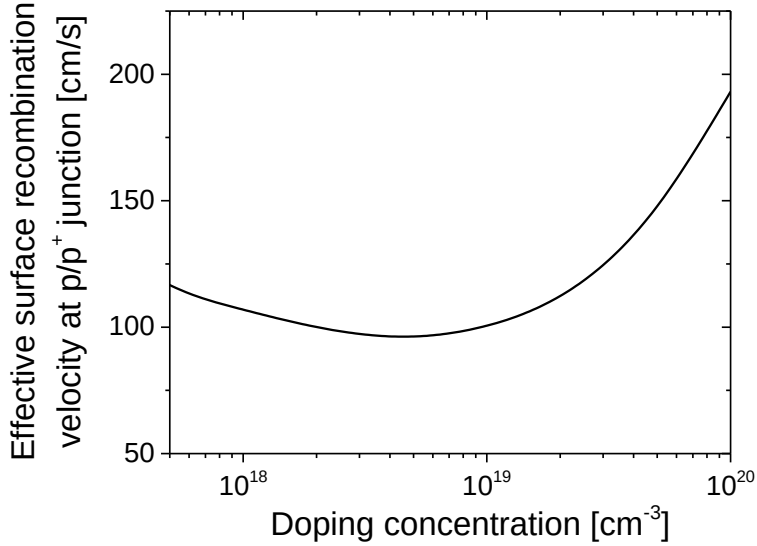

Figure 5. 2 The effective interface recombination velocity of a p/p⁺ high-low junction, as calculated based on eqns. (5.2)and (5.3). $N_{epi} = 10^{16}$ cm^{-3} and $S_{rear} = 10^4$ cm/s.

As explained earlier, the extraction of the bulk lifetime and the effective interface recombination velocity of such an asymmetrically-passivated bi-layer system (Figure 5. 1) is not a straight-forward task because the effect of the presence of the substrate on the measured signal must be removed from any measurement of the lifetime. Moreover, the dissimilar effective front and interface recombination velocities should be taken into account, where possible.

This effective lifetime can be expressed as [26]–[29]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{epi}} + \frac{1}{\tau_s} \tag{5.4}$$

with

$$\frac{1}{\tau_s} = \alpha_0^2 D_{epi} \tag{5.5}$$

where α_0 is the smallest eigenvalue of the transcendental equation

$$\tan(\alpha_0 d_{epi}) = \frac{S_{fr} + S_{int}}{\alpha_0 D_{epi} - \frac{S_{fr} S_{int}}{\alpha_0 D_{epi}}} \tag{5.6}$$

which should be solved numerically or graphically. Obviously, the surface lifetime, τ_s, depends on the effective surface and effective interface recombination velocities, S_{fr} and S_{int} respectively as well as the diffusion coefficient, D_{epi}, which accounts for the transport of bulk-generated carriers to the surface and interface. Bolou and Bois [29] as well as Sproul [27] presented an identical method to solve this equation graphically in order to derive approximate expressions for the surface lifetime for different scenarios of surface recombination velocities. The same method is used to derive an expression for the case of a p/p⁺ epitaxial layer structure which has dissimilar effective surface and effective interface recombination velocities such that $S_{int} \gg S_{fr}$. However, in the derivation, S_{fr} is not neglected.

Since different epitaxial layer thicknesses may be used in the experiments, it is convenient to normalise the surface recombination velocities to obtain reduced surface recombination velocities, S_i^*, as dimensionless quantities [27]

$$S_i^* = \frac{S_i d_{epi}}{D_{epi}}, \qquad i = fr, int \tag{5.7}$$

Similarly, the normalised surface lifetime, τ_s^*, can be written as

$$\tau_s^* = \frac{\tau_s}{\tau_{s,min}} \tag{5.8}$$

where

$$\tau_{s,min} = \frac{1}{D_{epi}} \left(\frac{d_{epi}}{\pi}\right)^2 \tag{5.9}$$

$\tau_{s,min}$ refers to the characteristic diffusion time of bulk-generated carriers to reach the surface / interface for recombination.

A plot of the normalised surface lifetime, calculated based on eqn. (5.5) and (5.6), as a function of the reduced surface and interface recombination velocities is shown in Figure 5. 3. For very large values of S_{int}^*, the surface lifetime becomes independent of the exact value of the surface/interface recombination velocity and all the curves converge to a constant τ_s^* value of 4. Thus, in this regime, the surface lifetime is limited by the transport of carriers by diffusion to the surface for recombination and not by the surface recombination rate itself. For low to moderate values of S_{int}^*, the reduced surface lifetime can be fitted very well with a hyperbolic function as indicated in Figure 5. 3. Since the plot is in logarithmic scale, eqn. (5.5) can be re-expressed approximately as the sum of the constant function (for large S_{int}^*) and the hyperbolic function (for small to moderate S_{int}^*) as follows

$$\tau_s^* = 4 + \frac{\pi^2}{S_{int}^* + S_{fr}^*} \tag{5.10}$$

i.e.

$$\tau_s = \frac{4}{D_{epi}} \left(\frac{d_{epi}}{\pi}\right)^2 + \frac{d_{epi}}{S_{int} + S_{fr}} \tag{5.11}$$

Compared to the case when the surface and interface recombination velocities are identical [27], an additional factor of 4 appears in eqn. (5.11). In other words, the diffusion length in the case of a sample with dissimilar surface and interface recombination velocities (i.e. only one highly recombinative surface) is twice compared to that in a sample where both the surface and interface are highly recombinative in equal measure.

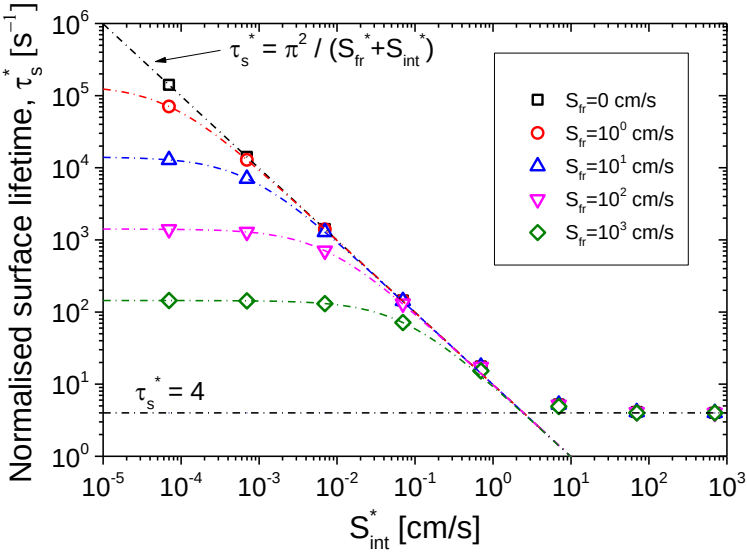

Figure 5. 3 Normalised surface lifetime plotted as function of different reduced surface and interface recombination velocities obtained from eqn. (5.5) and (5.6). Dashed lines represent hyperbolic functions and a constant function, indicated by the formulae.

Thus, the effective lifetime of the epitaxial film, as given by eqn. (5.4), can be re-expressed as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{epi}} + \frac{1}{\frac{d_{epi}}{S_{int}+S_{fr}} + \frac{4}{D_{epi}}\left(\frac{d_{epi}}{\pi}\right)^2} \tag{5.12}$$

However, for low to moderate interface recombination velocities, which is the case for an epitaxial layer on top of a pristine p^+ silicon substrate and an epitaxial layer on top of a BSF-shielded embedded porous silicon surface, a simplification can be made if

$$\frac{4}{D_{epi}}\left(\frac{d_{epi}}{\pi}\right)^2 \ll \frac{d_{epi}}{S_{int}+S_{fr}} = \frac{d_{epi}}{S_{tot}}$$

i.e.
$$\frac{S_{tot}d_{epi}}{D_{epi}} \ll \frac{\pi^2}{4} \tag{5.13}$$

or
$$S_{tot}^* \ll \frac{\pi^2}{4} \approx 2.47 \tag{5.14}$$

Under this condition, the diffusion-related term in eqn. (5.12) can be neglected i.e.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{epi}} + \frac{S_{int} + S_{fr}}{d_{epi}} \tag{5.15}$$

which is the commonly-known expression for the effective lifetime in terms of bulk lifetime and surface recombination velocities. This equation implies that the bulk lifetime of the epitaxial film and the sum of the surface and interface recombination velocities can be decoupled rather straight-forwardly by using a variation in the thickness of the epitaxial layers.

Among the many techniques that can be applied to measure the lifetime of attached epilayers, two techniques were studied in depth, namely, simulation-assisted steady-state photoluminescence (sim-PL) and microwave-detected photoconductance decay (μ-PCD) mainly because of the practical reason that these techniques were accessible either at IMEC or through established collaboration. The theoretical basis behind these techniques and their advantages and limitations are described in following sub-sections.

5.2.2 Simulation-assisted steady-state photoluminescence (sim-PL)

In one of the pioneering works in the efforts to measure the lifetime in attached epilayers, Rosenits *et al.* showed how lifetime of an epitaxial film can be extracted by combining photoluminescence (PL) measurements and modelling [8]. In this work, we will extend this method of simulation-assisted steady-state photoluminescence to extract both the bulk lifetimes and the effective interface recombination velocities of epitaxial layers deposited in areas with and without porous silicon.

Trupke *et al.* demonstrated the use of photoluminescence measurements in the quasi-steady state (QSSPL), transient (i.e. PL decay or PLD) and intermediate modes to measure the effective minority carrier lifetime in silicon wafers [30]. In this technique, radiative recombination in silicon is utilised to assess the level of excess carriers in an irradiated sample. At a similar time, Fuyuki *et al.* introduced electroluminescence (EL) imaging of silicon solar cells, where a small forward bias is applied to a finished solar cell in the dark and the luminescence distribution is captured with the acquisition of a single CCD camera image [31]. By means of calibration, this luminescence map can be converted to a minority carrier lifetime or diffusion length map, resulting in a spatially-resolved lifetime or diffusion length map that is acquired within seconds. Soon after, photoluminescence (PL) imaging (or mapping) was demonstrated by Trupke *et al.* [32]–[34] to evaluate silicon wafers at any process step. In contrast to QSSPL or PLD, PL imaging is a purely steady-state technique and is used for the work in this thesis.

5.2.2.1 Methodology for the extraction of bulk lifetime and effective interface recombination velocity

In our PL set-up, the sample is irradiated with a constant photon flux at 808 nm on the front side. This generates excess charge carriers, mostly within the epitaxial

layer, which recombine through various recombination pathways present in the epilayer. At steady-state, the generation of carriers, G, is balanced by a net recombination rate, U. The main recombination pathway that determines the excess carrier density level in the lowly-doped epitaxial silicon layer is Shockley-Read-Hall recombination (through bulk, surface or interface defects). Radiative recombination is present but at a much lower rate because silicon is an indirect band gap material. Under low-injection conditions, assuming no trapping effects (i.e. $\Delta n = \Delta p$), the radiative recombination rate, R_{rad} is directly proportional to the excess carrier density, Δn, since

$$\begin{aligned} R_{rad} &= B_{rad} np = B_{rad}(n_0 + \Delta n)(p_0 + \Delta n) \\ &= B_{rad}(n_0 + \Delta n)\big(N_{epi} + \Delta n\big) \\ &\cong B_{rad} N_{epi} \Delta n \end{aligned} \tag{5.16}$$

where B_{rad}, the coefficient of radiative recombination in silicon, is dependent on doping concentration, carrier concentration [35] as well as temperature [36] and N_{epi} is the doping level of the epitaxial layer. n_0 and p_0 are the thermal equilibrium carrier concentrations. Therefore, photons emitted due to radiative recombination can be used to probe the Δn level in the epitaxial layer and hence the lifetime.

The intensity of the photoluminescence, I_{PL}, is proportional to the depth-integrated radiative recombination rate and hence the depth-integrated excess carrier density [29], i.e.

$$\begin{aligned} I_{PL}(t) &= I_{PL}^{epi}(t) + I_{PL}^{sub}(t) \\ &= k \int_0^{d_{epi}} R_{rad}(x,t).\,dx + k \int_{d_{epi}}^{d_{tot}} R_{rad}(x,t).\,dx \end{aligned} \tag{5.17}$$

and if the substrate contribution to the measured PL signal can be neglected, then

$$I_{PL}(t) \cong \frac{k}{\tau_{rad,LLI}} \int_0^{d_{epi}} \Delta n(x,t).\,dx \tag{5.18}$$

where $\tau_{rad,LLI} = \frac{1}{B_{rad} N_{epi}}$ is the radiative lifetime of minority carriers in the epilayer in low injection, and k is the constant of proportionality accounting for the optical properties of the sample and hence is unknown and independent of the thickness of the epitaxial layer.

The excess carriers concentration profile in a p/p$^+$ silicon stack is simulated using PC1D [37] for different cases of epitaxial layer bulk lifetimes and thicknesses as shown in Figure 5. 4. When irradiated with an 808 nm laser, most of the photons are absorbed within the epitaxial layer for the range of thicknesses (20-50 µm) investigated in this thesis, since the absorption depth is only ~13 µm. Thus, the bulk of the carrier generation occurs within the epitaxial layer.

Moreover, the doping concentration of the epitaxial layer is 10^{16} cm^{-3}, three orders of magnitude lower than that of the substrate (10^{19} cm^{-3}). As a result, the substrate provides a back-surface field (BSF) which acts as a potential barrier for the minority carrier electrons diffusing from the epitaxial layer. Therefore, the

excess carrier density in the epitaxial layer is about ~2 orders of magnitude higher than that in the substrate near the interface with the epitaxial layer. The electron density further reduces very quickly deeper into the substrate due to diffusion and recombination. As such, the contribution of the substrate to the PL signal is much less in comparison to that of the epitaxial film. However, it should be pointed out that since $R_{rad} \cong B_{rad} N_A \Delta n$ (eqn. (5.16)), the high doping concentration in the substrate will enhance the level of radiative recombination and hence the PL signal from the substrate in the region around the epitaxial layer / p^+ substrate interface. Furthermore, the coefficient of radiative recombination is also diminished in a heavily-doped substrate and should be taken into account. Neglecting the PL signal from the substrate in the analysis would lead to a slight error in the evaluation of the epitaxial layer lifetime. Nevertheless, in the first instance, neglecting the substrate contribution to the PL signal in eqn. (5.18) is a reasonable approximation. A method to subtract the substrate PL signal from the measured signal will be treated towards in the next section.

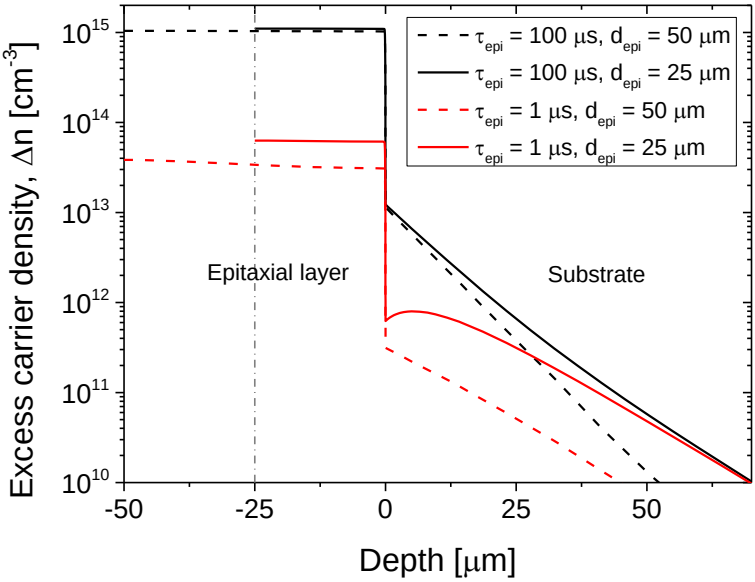

Figure 5. 4 Excess carrier density profiles simulated using PC1D [37] *for a p/p⁺ silicon stack assuming that the effective front surface and interface recombination velocities are ~10 cm/s and ~10³ cm/s respectively. The doping concentration of the epitaxial layer and the substrate are 10^{16} cm^{-3} and 10^{19} cm^{-3} respectively. The substrate lifetime is assumed to be 0.1 μs.*

Further to this, it is assumed that the effect of re-absorption of photons emitted by photoluminescence is negligible due to the large absorption depths (>150 μm) at long near-band gap wavelengths (>1000 nm). Trupke has shown this to be a reasonable assumption even for thick wafers [39]. It is also known that the dislocations in silicon produce a PL signal even at room temperature. This so-called D-band or defect luminescence occurs at a wavelength of ~1550 nm [33]. Since only silicon CCD cameras were used in this work, this PL signal will not affect the measured signal. This is illustrated in Figure 5. 5, which shows that the spectral

range of detected PL signal is between ~950-1100 nm. Porous silicon photoluminescence has also been reported in literature, with some PL bands occurring in the infrared range [40] where the lifetime measurements are made. However, such luminescence only occurs in as-etched porous silicon and is quenched by annealing and reorganisation of the pores into large voids [41] and hence it is not expected to influence the measurements either. Therefore, the measured PL signal in experiment is mainly due to the radiative recombination occurring in the epitaxial layer.

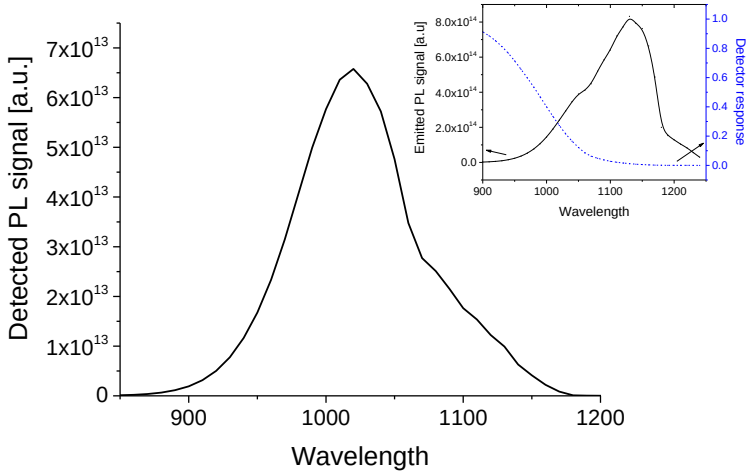

Figure 5. 5 The spectral range of detected PL signal using a silicon CCD camera is between ~950-1100 nm. Inset shows the emitted PL spectrum and the silicon sensor's response. The product of these two plots gives the detected PL spectrum. These curves were modeled using QSS-Model version 5.2 [38].

In order to calibrate the PL images resulting from the steady-state measurements and translate the PL intensities into average excess carrier densities and hence lifetime, the constant k in eqn. (5.18) must be found. The luminescence intensities of a PL image are usually calibrated using the industry-standard quasi-steady state photoconductance technique [3] to convert the PL intensity maps to lifetime maps. However, this is not possible for the p/p^+ structure due to the presence of the heavily-doped p^+ substrate. Rosenits et al. [8] described an elegant approach to do away with the need to find the unknown constant k: varying the epilayer thickness, d_{epi}, and taking ratios of PL signals between samples of two different thicknesses. From Figure 5. 4, we see that at a high bulk lifetime (100 µs), the excess carrier density is the same irrespective of the thickness of the epitaxial layer while the at low bulk lifetime (1 µs), the excess carrier density in the thicker epitaxial layer is lower compared to a thinner epitaxial layer that is irradiated with the same laser intensity. It is this difference that will be used in extracting bulk lifetime and/or sum of effective surface and interface recombination velocities from the PL maps by taking intensity ratios of sample of different epitaxial layer thicknesses.

This difference can be understood by considering the predominance of the bulk versus surface recombination. In an epitaxial layer with low bulk lifetime, volume recombination in the bulk predominates. Assuming that all incident photons are absorbed within the epitaxial layer, the greater volume of recombination centres in a thicker epitaxial layer results in a lower excess carrier density compared to a thinner epitaxial layer. On the other hand, for the epitaxial layers with high bulk lifetimes, it is the surface recombination that predominates and since the amount of surface does not change with the thickness of the epitaxial layer, the excess carrier density is independent of the thickness of the epitaxial layer.

From eqn. (5.18), we can express the ratio of PL intensities from samples of two different thicknesses as,

$$R_{d_1/d_2} = \frac{I_{PL,1}(t)}{I_{PL,2}(t)} = \frac{\int_0^{d_1} \Delta n(x,t)_1 . dx}{\int_0^{d_2} \Delta n(x,t)_2 . dx} = \frac{\Delta n_{av,1} . d_1}{\Delta n_{av,2} . d_2} \tag{5.19}$$

where the subscripts 1 and 2 denote two samples with different epitaxial layer thicknesses and Δn_{av} is the average excess carrier density in the epitaxial layer. By means of numerical simulations using PC1D [37], the excess carrier density profile, $\Delta n(z)$, in the p/p$^+$ stack can be obtained as shown in Figure 5. 4, for different epitaxial layer thicknesses and bulk lifetimes τ_{epi}, as well as different effective interface recombination velocities, S_{int}. With this, the fraction containing the integrals in eqn. (5.19) can be calculated for different assumed values of τ_{epi} and S_{int} for each pair of epitaxial layer thicknesses. What results is a set of calibration curves of R_{d_1/d_2} plotted against τ_{epi} for different S_{int} values, as shown in Figure 5. 6 for the epitaxial layer thickness pair of 20 and 80 μm. From experimental measurements of the PL intensities, the ratio of PL intensities in eqn. (5.19) can be calculated. Using such a chart and the experimentally-obtained ratios, we can read off τ_{epi} values for different assumed S_{int} values, as shown exemplarily in Figure 5. 6. A detailed explanation of how the method works can also be found in [8], [9].

As seen from Figure 5. 6, for relatively small S_{int} values of 10^2 or 10^3 cm/s, this method unambiguously leads to similar τ_{epi} values, more or less independent of the S_{int} values. However, when the interface recombination is high and S_{int} values are >10^3 cm/s, the calibration curves become sensitive to the actual value of S_{int}. Hence the τ_{epi} values that are extracted would depend strongly on the assumption made about S_{int}. So, different τ_{epi} values will result for each assumed value of S_{int} and it is not possible anymore to discriminate the two contributions with a single set of data. If, however, an appropriate additional constraint can be found, this sensitivity of the calibration curves to S_{int} is actually an advantage since it allows the determination of both the bulk lifetime and the effective interface recombination velocity in samples with rather high S_{int} such as an unshielded porous silicon-epilayer interface. In Chapter 6, two ways in which an additional constraint can be imposed on a family of solutions, (τ_{epi}, S_{int}), to arrive at the correct particular solution will be shown.

Several interesting observations can be made about the calibration curves in Figure 5. 6. Firstly, they have a sigmoidal shape albeit in a semi-log plot whereby at

low bulk lifetimes, the ratios are close to 1 and high bulk lifetimes, the ratios saturate at a constant value. Secondly, in the high S_{int} regime, the maximum PL ratio at large τ_{epi} values increases with S_{int}, in contrast to low S_{int} regime. Thirdly, the "inflection point" of these curves moves to smaller τ_{epi} values with increasing S_{int}. This last point can be understood by considering that as S_{int} increases, the critical bulk lifetime above which the effective lifetime no longer contains sufficient information about bulk recombination decreases. Thus, the higher the effective interface recombination velocity, the lower the maximum bulk lifetime that can be reliably extracted.

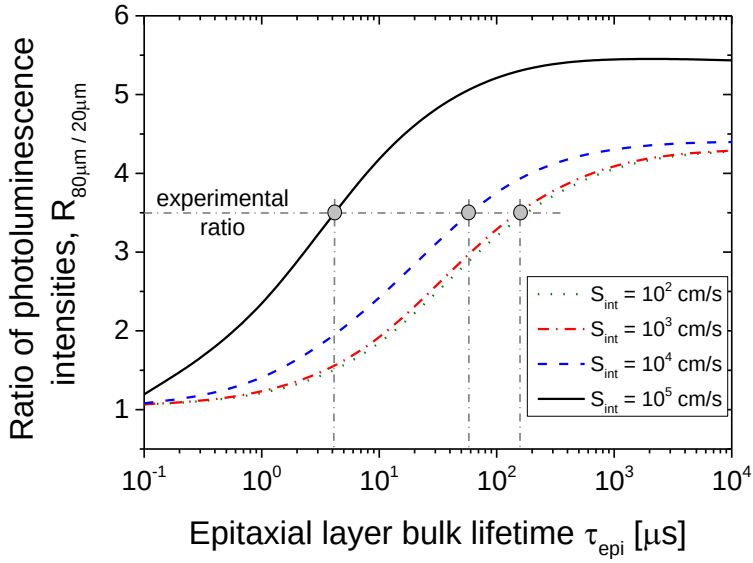

Figure 5. 6 Calibration curves plotting the ratio of the PL intensities from two samples with epitaxial layer thicknesses of 20 and 80 µm against different assumed τ_{epi} values, calculated based on PC1D simulations. For each S_{int} value, there is one calibration curve. The horizontal dash-dotted grey line represents an example of an experimentally-obtained PL intensity ratio, the intersection of which with each of the calibration curves gives graphical solutions, where we can read off τ_{epi} values from the horizontal axis for each S_{int}, leading to a family of solutions (τ_{epi}, S_{int}).

To understand the other observations, we relate the average excess carrier density level, Δn_{av}, in an epilayer to its effective lifetime. A remark that needs to be made at this juncture is that the effective lifetime associated with steady-state illumination, $\tau_{eff,steady}$ is in general different from that associated with transient illumination, $\tau_{eff,trans}$. However, under conditions of uniform photo-generation, small wafer (or in this case epilayer) thickness and low to moderate surface recombination velocities, $\tau_{eff,steady}$ and $\tau_{eff,trans}$ are virtually identical and so the transient equations that relate τ_{eff}, τ_{bulk} and S can also be used in steady-state analysis [42], with the only change being the π^2 pre-factor of the d_{epi}^2 term of eqn. (5.12) is replaced by 12 as has been reported in [43], [44] and derived in detail for

steady-state lifetime measurements by Turek in [45]. However, the error resulting from the use of equations based on transient illumination is rather negligible and so this correction can be neglected.

Let us first consider samples which satisfy the conditions (5.13) or (5.14), i.e. samples with $S \ll 10^4$ cm/s. In this case, the diffusion term in the expression for the surface lifetime can be neglected. This holds true for p/p⁺ silicon stacks without porous silicon and those where the porous silicon embedded in the p⁺ substrate is shielded by a BSF. Thus, we may use the simpler lifetime equation (eqn. (5.15)).

Under steady state conditions with uniform generation, where $G = U$, we can write

$$\Delta n_{av}\left(\frac{1}{\tau_{epi}} + \frac{S_{fr} + S_{int}}{d_{epi}}\right) = \frac{\phi_{ph}}{d_{epi}} \tag{5.20}$$

where ϕ_{ph} is the photon flux entering the epilayer and complete absorption by the epitaxial layer is assumed (i.e. large epitaxial layer thickness compared to absorption depth). This expression allows us to evaluate the dependence of Δn_{av} on the thickness d_{epi} of the epilayer. In the low lifetime regime $\left(\tau_{epi} \ll \frac{d_{epi}}{S_{tot}}\right)$, from eqn. (5.20), $\Delta n_{av} \propto \frac{1}{d_{epi}}$ and in the high lifetime regime $\left(\tau_{epi} \gg \frac{d_{epi}}{S_{tot}}\right)$, Δn_{av} is independent of d_{epi}.

Thus, from eqn. (5.19), the PL intensity ratios can be evaluated to be

$$R_{d_1/d_2} = \frac{\Delta n_{av,1}.d_1}{\Delta n_{av,2}.d_2} = \begin{cases} 1 \quad \text{if } \tau_{epi} \ll \dfrac{d_{epi}}{S_{tot}} \\ \dfrac{d_1}{d_2} \text{ if } \tau_{epi} \gg \dfrac{d_{epi}}{S_{tot}} \end{cases} \tag{5.21}$$

$$\text{where } S^*_{tot} \ll \frac{\pi^2}{4}$$

Result (5.21) can be verified against the curves corresponding to $S_{int} = 10^2$ and 10^3 cm/s in Figure 5. 6. For low τ_{epi} values, the ratios indeed converge towards 1, while at high τ_{epi} values, the ratios are given by the ratio of epilayer thicknesses. Moreover, for the cases where one of the epilayers is 20 μm thick, the ratios do exceed that predicted by the result (5.21). This is mainly due to the fact that photons of 808 nm have an absorption depth of ~13 μm and do not get fully absorbed in the 20 μm epitaxial layer, thereby increasing the ratios.

For samples with large S_{int}, conditions (5.13) or (5.14) are not satisfied and hence the diffusion term in eqn. (5.12) cannot be ignored. The d^2_{epi} dependence in this term becomes significant and at very high S_{int} values leads to $\Delta n_{av} \propto d$. Thus, in the worst case of S_{int} being close to the thermal velocity of ~10^7 cm/s, and neglecting the error introduced by using the transient equations, we get

$$R_{d_1/d_2} = \frac{\Delta n_{av,1}.\, d_1}{\Delta n_{av,2}.\, d_2} = \left(\frac{d_1}{d_2}\right)^2 \text{ if } \tau_{epi} \gg \tau_s \qquad (5.22)$$

This is why the maximum PL intensity ratios at large τ_{epi} values increase with S_{int}.

The calibration chart also indicates the limitations of this method in extracting bulk lifetimes: if the ratios are close to 1, or if the ratios are close to the higher limit predicted by the model, the intersection occurs in the flat portions of the chart which makes the uncertainty in the extraction of the bulk lifetime very high or the extraction itself impossible. This restricts the range of lifetimes for the epitaxial layers within which the bulk lifetimes can be reliably extracted. As already indicated, this range shifts to lower bulk lifetimes as S_{int} increases. Moreover, the calibration curves corresponding to samples with bigger thickness difference are better suited than ones with smaller thickness difference. However, practically, it is a challenge today to grow good quality epilayers thicker than 50 µm in a single epitaxial deposition. On the other hand, to have maximum absorption of light of 808 nm in the epilayer, it is better to have at least a 20 µm layer.

5.2.2.2 *Correction procedure for subtracting the substrate photoluminescence contribution*

The extraction method as exemplified in Figure 5. 6 holds true only as long as the experimental ratios calculated from the measured PL intensity maps are not significantly affected by PL signal emitted by the substrate. In this section, the extent of the influence of the substrate on the measured signal is analysed and a method to correct the substrate PL signal is proposed.

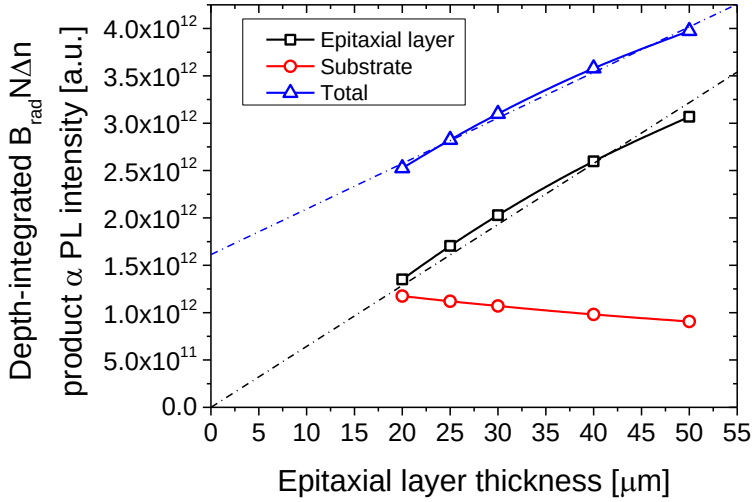

Figure 5. 7 The depth-integrated $B_{rad}N\Delta n$ product, which is proportional to the PL intensity as given in eqn. (5.17) is plotted for different epitaxial layer thicknesses. These simulations were done for an epitaxial layer with a bulk lifetime of 100 µs. All other parameters are similar to those used in Figure 5. 4.

In order to evaluate the contribution of the substrate to the measured PL signal, the integrals associated with both the epitaxial layer and the substrate in eqn. (5.17) were calculated from carrier density profiles obtained from PC1D simulations similar to that of Figure 5. 4. This is done by plotting the product $B_{rad}N\Delta n$ as a function of depth and calculating the area under the graphs. Here, N is the depth-dependent doping concentration and B_{rad} depends on the doping concentration. Figure 5. 7 shows the depth-integrated $B_{rad}N\Delta n$ product calculated from PC1D simulations for the typical case of an epitaxial layer with a bulk lifetime of 100 μs and substrate doping concentration of 10^{19} cm^{-3}, for various epitaxial layer thicknesses.

There appears to be a non-negligible contribution of the substrate towards the total PL signal measured from the sample. This will reflect as a non-zero intercept to the PL intensity-axis for data measured in an experiment, as illustrated in Figure 5. 7 for total PL intensity curve. Note that the linear fit lines serve the purpose as guides for the eye so as to illustrate the substrate contribution. In general, the plots are non-linear functions. If this substrate contribution is not corrected before the PL intensity ratios are calculated, it can result in an under-estimation of the bulk lifetime using the method explained in Figure 5. 6.

In order to correct the substrate PL contribution and to understand what factors influence the fraction of PL signal coming from the substrate, it is useful to model the excess carrier density curves of Figure 5. 4 analytically, both in the epitaxial layer and in the substrate.

Consider the p/p$^+$ structure as depicted in Figure 5. 1 without the embedded porous silicon layer. The case of epitaxial layer with an embedded porous silicon layer will be treated subsequently. The various parameters recalled in the following derivations are explained in the text and caption around Figure 5. 1. Two depth axes have been defined, namely x and x'. This is because the excess carrier density profiles for the epitaxial layer and substrate will be derived separately from a general solution, making it convenient to use axes with different origins.

In the general case of a p-type silicon sample (with parameters τ, L, D) irradiated with monochromatic light (fixed absorption coefficient, α) with a constant flux density, ϕ_0, producing a non-uniform generation profile, $G(x)$, within the sample, the excess minority carrier density, $\Delta n(x)$, can be obtained from the solution of the one-dimensional (1D) continuity equation [46]

$$D\frac{d^2\Delta n(x)}{dx^2} - \frac{\Delta n(x)}{\tau} + G(x) = 0 \tag{5.23}$$

with

$$G(x) = \phi_0\alpha(1-R)e^{-\alpha x} \tag{5.24}$$

where R is the reflectivity at the surface of the sample. Depletion approximation is assumed whereby there are no electric fields outside the space-charge region associated with the p/p$^+$ junction between epitaxial layer and the substrate, which allows us to neglect drift terms of the continuity equation. In addition, each absorbed photon is assumed to produce one electron-hole pair (ehp). Furthermore, it is assumed that the illumination area is much larger than the minority carrier diffusion lengths, and so the problem can be reduced to 1D.

The general solution to eqn. (5.23) and (5.24) has been derived by Hovel in [47] as follows

$$\Delta n(x) = A\cosh\left(\frac{x}{L}\right) + B\sinh\left(\frac{x}{L}\right) - Ce^{-\alpha x} \tag{5.25}$$

with

$$C = \frac{\phi_0\alpha(1-R)\tau}{\alpha^2L^2 - 1} \tag{5.26}$$

and

$$L = \sqrt{D\tau} \tag{5.27}$$

A and B are constants to be found with appropriate boundary conditions for the epilayer and for the substrate.

For the case of the epilayer, the following boundary conditions apply.

$$\left.\frac{d\Delta n(x)}{dx}\right|_{x=0} = S_{fr}\frac{\Delta n(0)}{D_{epi}} \tag{5.28}$$

and

$$\left.\frac{d\Delta n(x)}{dx}\right|_{x=d_{epi}^-} = -S_{int}\frac{\Delta n(d_{epi}^-)}{D_{epi}} \tag{5.29}$$

With these boundary conditions, the excess carrier density profile in the epitaxial layer can now be expressed as [46], [48]

$$\Delta n_{epi}(x) = C\left[\frac{A_1 + B_1\mathrm{e}^{-\alpha d_{epi}}}{D_1} - \mathrm{e}^{-\alpha x}\right] \tag{5.30}$$

where

$$A_1 = \left(\frac{S_{fr}S_{int}L}{D} + S_{int}\alpha L\right)\sinh\left(\frac{d_{epi}-x}{L}\right) + \left(S_{fr} + \alpha D\right)\cosh\left(\frac{d_{epi}-x}{L}\right)$$

$$B_1 = \left(\frac{S_{fr}S_{int}L}{D} - S_{int}\alpha L\right)\sinh\left(\frac{x}{L}\right) + \left(S_{int} - \alpha D\right)\cosh\left(\frac{x}{L}\right)$$

$$D_1 = \left(\frac{S_{fr}S_{int}L}{D} + \frac{D}{L}\right)\sinh\left(\frac{d_{epi}}{L}\right) + \left(S_{fr} + S_{int}\right)\cosh\left(\frac{d_{epi}}{L}\right)$$

In eqn. (5.30), L denotes L_{epi} (the minority carrier diffusion length in the epitaxial layer) and D denotes D_{epi} (the minority carrier diffusion coefficient in the epitaxial layer).

A significant simplification to the complex formulation of eqn. (5.30) can be made by recognising that the absorption coefficient of long wavelength irradiation is small enough to result in an approximately uniform generation profile within the epitaxial layer. Therefore, the diffusion term in eqn. (5.23) can be dropped, leading to an excess carrier density profile that is uniform (see also eqn. (5.20))

$$\Delta n_{epi} = G_{av}\tau_{eff} = \frac{\phi_0(1-R)}{d_{epi}}\tau_{eff} \tag{5.31}$$

Now, for the substrate, in formulating the boundary conditions for the solution of excess carrier concentration, it is important to recognise that the excess carrier concentration in the substrate, unlike that in the epitaxial layer, is contributed by not only photo-generation, but also by the injection of the minority carriers from the epitaxial layer over the p/p^+ barrier into the substrate. It is of paramount

importance that one of the boundary conditions captures this phenomenon. In particular, since there is a high-low junction at the interface, the minority carrier density on either side of the space charge region will be related, taking into account the built-in potential which determines the excess minority carrier density injected into the substrate from epitaxial layer [20], [49]. Assuming that the quasi-Fermi levels are constant across the space charge region and the built-in potential is the same as at thermal equilibrium, the boundary conditions for the interface and the rear can be written as

$$\Delta n_{sub}(0^+) = \Delta n_{epi}(0^-)\mathrm{e}^{\frac{-q\psi_{bi}}{k_B T}} \tag{5.32}$$

and

$$\left.\frac{d\Delta n(x')}{dx'}\right|_{x'=d_{sub}} = -S_{rear}\frac{\Delta n(d_{sub})}{D_{sub}} \tag{5.33}$$

where

$$\psi_{bi} = \frac{k_B T}{q}\ln\left(\frac{N_{sub}}{N_{epi}}\right) - \frac{\Delta E_{G,sub}}{q} \tag{5.34}$$

The built-in potential which regulates the amount of minority carriers injected into the substrate is reduced by BGN as indicated in eqn. (5.34). Notice that the x' coordinate is now used in the subsequent derivations.

Applying the boundary conditions (5.32) and (5.33) to the general solution (5.25) results in the following expression for the excess carrier density profile in the substrate:

$$\Delta n_{sub}(x') = A_2\cosh\left(\frac{x'}{L}\right) + B_2\sinh\left(\frac{x'}{L}\right) - C_2 e^{-\alpha x'} \tag{5.35}$$

with

$$C_2 = \left(\frac{\phi_0\alpha(1-R)\tau_{sub}}{\alpha^2 L_{sub}^2 - 1}\right)\mathrm{e}^{-\alpha d_{epi}}$$

$$A_2 = \Delta n_{epi}(0^-)\frac{N_{epi}}{N_{sub}}\mathrm{e}^{\frac{\Delta E_{G,sub}}{k_B T}} + C_2$$

$$B_2 = \frac{C_2\left(\frac{S_{rear}}{D_{sub}} - \alpha\right)\mathrm{e}^{-\alpha d_{sub}} - A_2\left[\frac{1}{L_{sub}}\sinh\left(\frac{d_{sub}}{L_{sub}}\right) + \frac{S_{rear}}{D_{sub}}\cosh\left(\frac{d_{sub}}{L_{sub}}\right)\right]}{\frac{S_{rear}}{D_{sub}}\sinh\left(\frac{d_{sub}}{L_{sub}}\right) + \frac{1}{L_{sub}}\cosh\left(\frac{d_{sub}}{L_{sub}}\right)}$$

Note the factor $\mathrm{e}^{-\alpha d_{epi}}$ in C_2 accounts for the fact that the intensity of light reaching the substrate is diminished by the absorption in the epitaxial layer.

The analytical models for the excess carrier density in the epitaxial layer and the substrate that have been derived so far (see eqns. (5.30)and (5.35)) have been plotted in Figure 5. 8 for 50 µm-thick epitaxial layers of two different bulk lifetimes (1 and 100 µs). Numerical simulations using PC1D of the same structure and parameters are also plotted for comparison. The analytical models fit the numerical simulations perfectly and can therefore be used as the basis for correcting the substrate contribution to the measured PL intensity.

As explained before, the excess carriers in the substrate are due to both photo-generation and injection of excess carriers from the epitaxial layer into the

substrate. The amount of photo-generation depends on the thickness of the epitaxial layer, the intensity of irradiation and the wavelength of the photons. The amount of carrier injection over the p/p⁺ barrier depends on the barrier potential and the minority carrier lifetime in the epitaxial layer. An epitaxial layer with a higher minority carrier lifetime will lead to a higher density of excess carriers in the epitaxial, which in turn results in a greater drain of carriers into the substrate. Needless to say, when the barrier potential is lowered, by reducing the doping concentration difference between the epitaxial film and the substrate, there will be greater injection of minority carriers over the barrier.

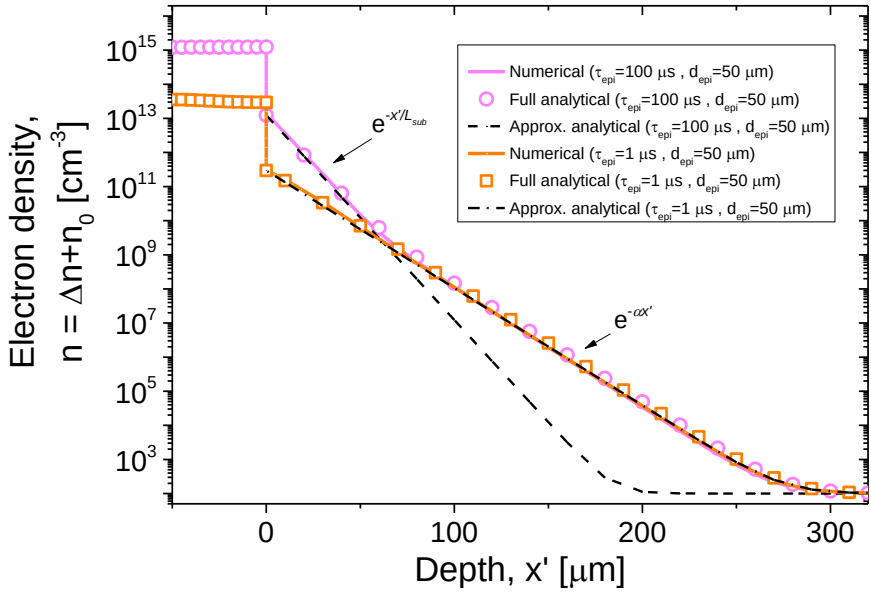

Figure 5. 8 Excess carrier density profiles plotted for 50 μm thick epitaxial layers for two different bulk lifetimes (1 and 100 μs) showing a comparison of the derived analytical models (based on eqns. (5.30)and (5.35)) with numerical simulations based on PC1D. While the numerical simulation results are plotted as solid lines (orange and light magenta respectively), the results from the calculations based on the analytical models are plotted as scatter points of the same colour. The analytical model fits the numerical simulations almost perfectly. Simplified approximate models for the excess carrier density in the substrate are also plotted as black, dash-dotted and dashed lines.

When the injection of excess carriers over the high-low junction dominates over the photo-generation in the substrate (which is most often the case, except for very low lifetime epitaxial layers), the reduction in the excess carrier density with depth in the regions close to the interface of the substrate is dominated by the minority carrier diffusion length (L_{sub}) in the substrate. Deeper in the substrate, where photo-generation dominates, reduction in the excess carrier density is characterised by the absorption length (α^{-1}). This can be clearly observed from the exponential fits ($e^{-x'/L_{sub}}$ and $e^{-\alpha x'}$) in Figure 5. 8. For the case of the 100 μs epitaxial layer, the initial excess carrier density reduction has a slope of $-1/L_{sub}$ in a semi-log plot, while deeper in the substrate this reduction has a slope of $-\alpha$. On

the other hand, in the case of the low lifetime sample (1 μs), the profile has a slope of $-\alpha$ throughout. This is because, in a low lifetime epitaxial layer, the excess carrier density is low and hence the injection across the barrier is comparable to or lower than the photo-generation rate in the substrate.

Based on these observations and understanding, useful simplifications can be made to the complex form of eqn. (5.35). Before that, two cases must be distinguished, one where the excess carrier density close to the interface is dominated by excess carriers injected over the high-low barrier, and another which is dominated by photo-generation.

When injection of excess carriers from the epitaxial layer is the main source of minority carriers on the substrate side compared to the contribution from photo-generation of carriers (i.e. high lifetime epitaxial layer and/or large diffusion length in substrate), the generation term in eqn. (5.23) can be dropped. Furthermore, assuming that the thickness of the substrate is much larger than the minority carrier diffusion length (i.e. $d_{sub} \gg L_{sub}$), the following simple equation can be derived for the excess carrier density profile in the substrate

$$\Delta n_{sub}(x') = \Delta n_{epi}(0^-)\frac{N_{epi}}{N_{sub}}\mathrm{e}^{\frac{\Delta E_{G,sub}}{k_B T}}\mathrm{e}^{-\frac{x'}{L_{sub}}} \tag{5.36}$$

This is plotted in Figure 5. 8 as the approximate analytical model for the high lifetime (100 μs) epitaxial layer. Although the fit is excellent only for the initial part of the profile and diverges from the numerical simulations deeper in the substrate, it is not critical since the quantity of interest is actually the area under the curve (which is proportional to the substrate PL intensity, assuming B_{rad} and N are constant in the substrate). The area under the curve for the approximate model differs only by ~2.1% compared to the full analytical or numerical model (due to the log scale of the vertical axis). Therefore, this approximate equation can be used for the case of high lifetime epitaxial layers and/or large minority carrier diffusion length in substrate, where the excess carrier density profile (at least close to the interface region) is dominated by L_{sub}.

On the other hand, for the case when the excess carrier density profile is dominated by photo-generation (i.e. low lifetime epitaxial layer and/or small diffusion length in the substrate), the factor C_2 in eqn. (5.35) dominates the injection-related terms. As a result, this equation can be simplified to describe the excess carrier density in the substrate as

$$\Delta n_{sub}(x') = -C_2\mathrm{e}^{-\alpha x'} = \left(\frac{\phi_0\alpha(1-R)\tau_{sub}}{1-\alpha^2 L_{sub}^2}\right)\mathrm{e}^{-\alpha d_{epi}}\mathrm{e}^{-\alpha x'} \tag{5.37}$$

This is plotted as the approximate analytical model in Figure 5. 8 for the case of the low lifetime (1 μs) epitaxial layer. It is interesting to note that this approximate equation is dependent on the thickness of the epitaxial layer but not the excess carrier density in the epilayer.

For the first case (injection-dominated excess carrier profile in substrate), the average excess carrier density in the epitaxial layer and the excess carrier density at the edge of the space-charge region in the substrate are related (see eqns. (5.31), (5.32) and (5.36)). Thus, it is possible to calculate the contribution of the substrate

to the PL intensity if the parameters of the substrate (doping concentration and diffusion length) are known, without having the knowledge about the exact excess carrier density level and/or the bulk lifetime in the epitaxial layer beforehand. This becomes apparent when the substrate PL intensity is expressed as a fraction of the total PL intensity from the sample i.e.

$$\overline{I_{PL}^{sub}} = \frac{I_{PL}^{sub}}{I_{PL}^{tot}} = \frac{\int_{d_{epi}}^{d_{tot}} B_{rad}^{sub} N_{sub} \Delta n_{sub}.dx}{\int_{0}^{d_{epi}} B_{rad}^{epi} N_{epi} \Delta n_{epi}.dx + \int_{d_{epi}}^{d_{tot}} B_{rad}^{sub} N_{sub} \Delta n_{sub}.dx} \tag{5.38}$$

For epitaxial layers with a high bulk lifetime (e.g. >50 µs for a substrate with doping concentration of 10^{19} cm^{-3}), eqns. (5.31) and (5.36) are applicable. Furthermore, assuming that $d_{sub} \gg L_{sub}$, eqn. (5.38) becomes

$$\overline{I_{PL}^{sub}} = \frac{B_{rad}^{sub} L_{sub} \mathrm{e}^{\frac{\Delta E_{G,sub}}{k_B T}}}{B_{rad}^{epi} d_{epi} + B_{rad}^{sub} L_{sub} \mathrm{e}^{\frac{\Delta E_{G,sub}}{k_B T}}} \tag{5.39}$$

This expression implies that the fractional contribution of the substrate towards the measured PL intensity depends *only* on the substrate parameters (namely, doping concentration and minority carrier diffusion length) *if* the epitaxial layer thickness and doping are known. Furthermore, the fraction does *not* depend on the excess carrier concentrations. This is a very important result because this allows the substrate PL contribution to be corrected from the measured signal without knowing the excess carrier densities in the sample beforehand.

Figure 5. 9 plots the fractional contribution of the substrate to the measured PL intensity for different substrate doping concentrations, which in principle should be valid for a variety of samples with different epitaxial layer lifetimes and barrier ratios, so long as the excess carrier density in the substrate is injection-dominated. Firstly, as expected, the substrate contribution to the measured PL is higher for thinner epitaxial layers, not only because of increased photo-generation but also because of increased injection of carriers over the high-low junction in thinner epitaxial layers which have higher excess carrier density for the same bulk lifetime. Secondly, it can also be observed that as the substrate doping concentration increases, the PL contribution from the substrate decreases. This is attributed to the lower minority carrier diffusion lengths in more heavily-doped substrates. A plot of the fractional contribution of the substrate to the measured PL intensity calculated from numerical simulations using PC1D for a 100 µs epitaxial layer is also shown in Figure 5. 9 which shows that the analytical model based on eqn. (5.39) slightly underestimates the substrate contribution, especially for thinner epitaxial layers. However, this difference can be neglected since the convenience in the use of the elegant expression of eqn. (5.39) outweighs the error.

Therefore, by knowing the doping concentration of the substrate, and assuming that the diffusion length is limited by Auger recombination, the fractional contribution of the substrate to the measured PL intensity can be calculated for each epitaxial layer thickness and the measured PL intensity can thus be corrected during experiments. This procedure is illustrated in Figure 5. 10 for a substrate

with a doping concentration of 10^{19} cm^{-3} for three different epitaxial layer bulk lifetimes. The plots are similar to that of Figure 5. 7, with an additional plot labelled as "Total (after correction)" showing the result after the correction procedure based on eqn. (5.39) has been applied on the plot labelled "Total" which corresponds to what would be measured in an experiment. For the epitaxial layers with 100 µs and 50 µs, the correction procedure works very well since the "Total (after correction)" plots almost coincide with "Epilayer" plots. A slight underestimation of the PL signal from the substrate is observed at smaller epitaxial layer thicknesses. This is because from thinner epitaxial layers, photo-generation in the substrate becomes more important.

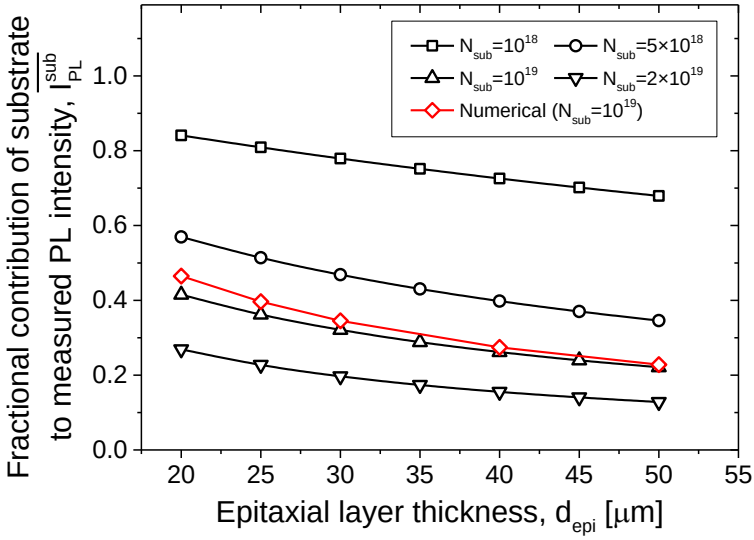

Figure 5. 9 The fractional contribution of the substrate to the measured PL intensity, calculated based on eqn. (5.39), is plotted for samples of different epitaxial layer thicknesses and four different cases of substrate doping concentrations, namely 10^{18} cm^{-3} ($L_{sub} = 84.67$ µm), 5×10^{18} cm^{-3} ($L_{sub} = 15.16$ µm), 10^{19} cm^{-3} ($L_{sub} = 7.23$ µm) and 2×10^{19} cm^{-3} ($L_{sub} = 3.49$ µm). A plot of this quantity, calculated based on numerical simulations using PC1D, for the case of a substrate with a doping concentration of 10^{19} cm^{-3} and an epitaxial layer with a bulk lifetime of 100 µs is also shown for comparison.

For the case of the epitaxial layer with a bulk lifetime of 10 µs, it can be observed that the "Total" PL intensity that would be measured during experiments will decrease with increasing epitaxial layer thickness. This is already a clear indication that the measured PL intensity is significantly dominated by the substrate PL. However, the described correction procedure does not work well for this case, and there is significant underestimation of the substrate PL, which increases significantly for thinner epitaxial layers. Using eqn. (5.37) to derive the fractional substrate contribution of substrate towards the total PL intensity will not work because it will require prior knowledge about the excess carrier densities in the samples. Thus, it is clear that the correction procedure based on eq. (5.39)

only works if the epitaxial layer bulk lifetime is at least ~50 µs when the epitaxial layer is grown on a substrate with a doping concentration of 10^{19} cm^{-3}.

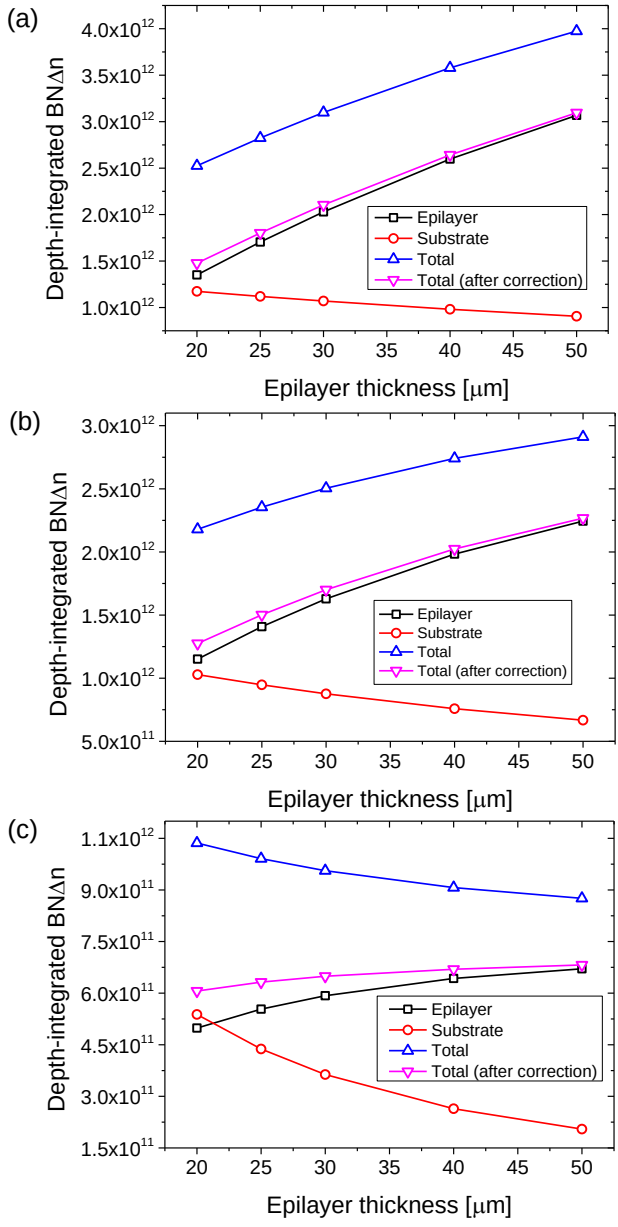

Figure 5. 10 The depth-integrated $B_{rad}N\Delta n$ product, which is proportional to the PL intensity as given in eqn. (5.17) is plotted for different epitaxial layer thicknesses. These simulations were done for an epitaxial layer with a bulk lifetime of (a) 100 µs, (b) 50 µs and (c) 10 µs. All other parameters are same as those used in Figure 5. 4. The plot corresponding to "Total (after correction)" is the result after the plot labelled "Total" has been corrected using eqn. (5.39).

However, in low lifetime samples, where the substrate excess carrier density is dominated by photo-generation, the substrate contribution can be corrected rather straight-forwardly by simply measuring the PL intensity on a passivated substrate without the epitaxial layer and multiplying it with a factor of $e^{-\alpha d_{epi}}$ to account for the absorption if an epitaxial layer would be present and subtracting this from the measurement on an epitaxial layer sample. The corrected PL then corresponds to substrate PL contribution when there is no injection of excess carriers over the high-low barrier. Thus, in a sample completely dominated by photo-generation with very little injection, the substrate PL can be corrected directly in this way.

There are two more ways in which the correction errors in Figure 5. 10 can be completely eliminated by: (1) using a laser with a shorter wavelength (e.g. 532 nm) and (2) reducing the barrier ratio, for example, by using a substrate with a lower doping concentration. For the latter case, note that the injection across the barrier is influenced by BGN (see Figure 5. 2). Nevertheless, since the minority carrier diffusion length in a lower-doped substrate is higher (assuming Auger-limited lifetime), the excess carrier profile will then be injection-dominated.

Finally, we consider the situation where there is a porous silicon layer embedded on the substrate side of the p/p^+ junction. The interface of such a sample is highly-recombinative owing to the fact that there is a large internal area of unpassivated void surfaces. Thus, the excess carrier density in the substrate close to the interface with the epitaxial layer must be very low, compared to the case without the embedded porous silicon. Since the excess carrier concentration drops steeply with depth into the substrate, it is in fact the substrate region close to the interface that contributes to the measured PL signal. PL signal from deeper in the substrate is negligible compared to that from the epitaxial layer. Thus, we can expect that in samples with embedded porous silicon, the PL signal from the substrate will be largely suppressed due to the highly-recombinative interface region.

In general, such a structure is difficult to model using PC1D because the optical properties of porous silicon (reflectance, scattering, etc.) must be taken into account and will affect the accuracy of the calculations to estimate the fractional contribution of the substrate to the measured PL signal. However, as a first approximation, these phenomena are excluded in the PC1D simulation results shown in Figure 5. 11. In this case, the porous silicon layer is modelled as a region inside the p^+ silicon substrate with diffusion length in the order of the distance between the voids in the porous silicon i.e. ~100 nm with the interface recombination velocities between this region and surrounding silicon limited by the thermal velocity of 10^7 cm/s.

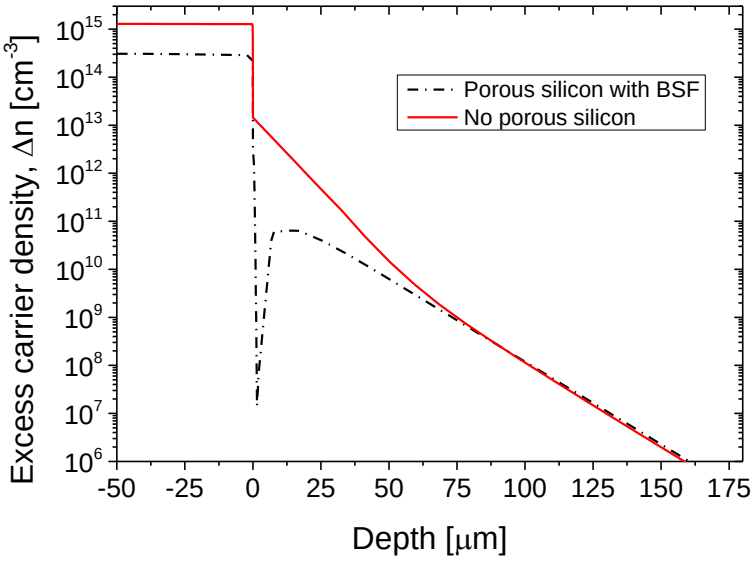

Figure 5. 11 Excess carrier density profiles for an epitaxial layer with a bulk lifetime of 100 μs. For the case with porous silicon, only the electrical properties of porous silicon is taken into account. The minority carrier diffusion length in porous silicon is assumed to be in the order of the inter-void distance of ~100 nm, while the recombination velocities of the interface of its regions with surrounding silicon is taken to be limited by thermal velocity of 10^7 cm/s. Other parameters are similar to the ones in Figure 5. 4.

The excess carrier concentration in the substrate especially at the interface region is severely diminished compared to the case without an embedded porous silicon layer (also shown in Figure 5. 11 for comparison). This would mean that the contribution of substrate to the measured PL intensity is negligible. In this particular case of an epitaxial layer with a 100 μs bulk lifetime protected from the porous silicon by a 1 μm thick BSF of the same doping concentration as the substrate (10^{19} cm^{-3}), the substrate contribution would be only ~2% even if we assume 100% transmission and no scattering through the porous silicon layer for the substrate PL photons. Thus, we expect that a linear extrapolation to $d_{epi} = 0$ μm in a plot like that of Figure 5. 7 for the measured PL intensity on samples with porous silicon should intersect at the origin. In this case, the sim-PL method described in this section is valid for porous silicon samples, and no correction of the measured PL intensities would be necessary.

5.2.3 Microwave-detected photoconductance decay (μ-PCD)

5.2.3.1 Measurement methodology

The most straight-forward method to measure the effective minority carrier lifetime of an epitaxial film is microwave-detected photoconductance decay (μ-PCD), which is a transient decay method [43]. In this technique, an infrared laser with a wavelength of 904 nm (for all work presented in this chapter) and pulse

duration of 200 ns is used to excite the wafer and generate electron-hole pairs. After the pulsed excitation, the concentration of excess carriers decays to the equilibrium minority carrier concentration. The time constant of the fundamental mode of decay can be measured using the reflection of a microwave probe signal whose frequency is tuned between 10 and 10.5 GHz so as to obtain the highest sensitivity while maintaining good linearity between measured signal and the conductivity. When certain conditions are met, the change in the reflected power of the microwave signal will be proportional to the change in conductivity of the sample [50]–[52], i.e.

$$\frac{\Delta P_R}{P_R(\sigma_0)} = \frac{1}{R(\sigma_0)}\left(\frac{\partial R(\sigma)}{\partial \sigma}\right)_{\sigma=\sigma_0} \Delta\sigma = A(\sigma_0)\Delta\sigma \tag{5.40}$$

where σ_0 is the dark conductivity of the sample, $P_R(\sigma_0)$ is the reflected microwave power in dark conditions, $\Delta P_R = P_R(\sigma_0 + \Delta\sigma) - P_R(\sigma_0)$ is change in reflected microwave power due to the additional conductivity, $\Delta\sigma$, resulting from the generated excess carriers, $R(\sigma)$ is the reflection coefficient (the ratio between reflected power and incident power) and $A(\sigma_0)$ is the sensitivity factor.

The excess conductivity is proportional to the excess carrier density, Δn (or Δp). As the excess carrier density decays, the conductivity drops and this causes a change in the reflected microwave power. The time constant of the decay is usually calculated with a mono-exponential fit around tail part of the transient (i.e. the fundamental decay mode) where the slope of the decay is approximately linear in a semi-logarithmic plot of the sensed signal versus time [26], [29]. A time constant extracted in this way is referred to as the "asymptotic effective lifetime" or "apparent lifetime". This time constant will contain information about both the bulk lifetime and surface / interface recombination velocities of the epitaxial film.

5.2.3.2 Influence of the substrate on the measurement

In order to understand if μ-PCD measurements are influenced significantly by the presence of the p⁺ substrate, we will consider the normalised intensity of the microwave probe signal entering the sample [53], [54]

$$w(x) = e^{\left(-\frac{x}{\delta}\right)} \tag{5.41}$$

where $\delta = \sqrt{\frac{\rho}{\pi\nu\mu_r\mu_0}}$ is the skin depth of the microwave due to free carrier absorption in silicon. ρ is the resistivity of the sample, ν is the frequency of the microwave signal and μ_r and μ_0 are the relative permeability of the sample and absolute permeability of vacuum, respectively. The apparent average carrier density, Δn_{app}, sensed by the microwave probe signal penetrating an epitaxial sample with p/p⁺ structure at any given time, t, can be expressed as

$$\Delta n_{app}(t) = \frac{\int_0^{d_{epi}} C\left(\sigma_{0,epi}\right)\Delta n(x,t).\, w(x).\, dx}{\int_0^{d_{epi}} w(x).\, dx} \tag{5.42}$$

$$+\frac{\int_{d_{epi}}^{d_{tot}} C(\sigma_{0,sub})\Delta n(x,t).w(x).dx}{\int_{d_{epi}}^{d_{tot}} w(x).dx}$$

The first term on the right-hand side (RHS) in eqn. (5.42) is associated with signal from the epitaxial layer, while the second term accounts for the influence of the substrate on the measurement. Here, the intensity of the microwave probe signal, $w(x)$ is used as a weighting factor. The constants $C(\sigma_{0,epi})$ and $C(\sigma_{0,sub})$ account for the fact that the sensitivity of the reflected microwave signal is dependent on the conductivity of the layer. If the second term is small compared to the first term, then the apparent excess carrier density will be representative of the excess carrier density in the epitaxial film.

The normalised intensity of a ~10.3 GHz microwave probe signal penetrating an epitaxial layer with a resistivity of 3 Ω.cm on top of a highly-doped p^+ substrate with a resistivity of ~0.001 Ω.cm is plotted in Figure 5. 12. In the epitaxial layer, the skin depth is ~857 μm, while in the highly-doped substrate, the skin depth is only ~16 μm. Thus, the microwave signal is strongly attenuated in the substrate. As a result, the penetrating wave is strongly confined within the epitaxial layer and the second term in the RHS of eqn. (5.42) is largely diminished compared to the first term. Thus, the measured signal is largely representative of the excess carrier density decay in the epitaxial layer.

Secondly, as mentioned earlier, the sensitivity of the microwave reflectance to changes in conductivity depends on the conductivity itself. At high conductivities, similar to that in the highly-doped p^+ substrates used in this work, the sensitivity is nearly zero, as reported by Schöfthaler and Brendel [55]. Thus, the resulting microwave signal will not be sensitive to changes in conductivity in the substrate.

Finally, Walter *et al.* [5] have reported simulations of excess carrier decay curves in a p/p^+ structure after a pulsed excitation representative of the μ-PCD measurement set-up used in this work. These curves show a strong initial decay that later stabilises to a constant slope from which the fundamental effective lifetime can be extracted. This strong initial decay has been attributed to the changes in excess carrier density in the substrate and near the interface between the epitaxial layer and the substrate, rather than the front surface recombination, because the epitaxial layer is rather thin. The substrate lifetime is assumed to be Auger-limited [16], [56] due to the heavy doping. Due to the low lifetime in the substrate compared to the epitaxial film, the decay associated with the substrate occurs at the beginning of the transient, while the asymptotic decay corresponds only to the excess carrier decay in the epitaxial layer. The method proposes to fit the tail of the curve. Thus, the effective lifetimes measured using μ-PCD method represent that in the epitaxial film.

It should be noted, however, that the strong initial decay that has been simulated could not be observed experimentally [5], neither in literature nor in this work, possibly because of the poor penetration of microwaves into the substrate and the poor sensitivity of the signal to changes in substrate conductivity. An alternative explanation is that this decay happens too quickly at the beginning

of the transient that it is hardly observable in experiment. This will be further discussed together with measurement results in Chapter 6.

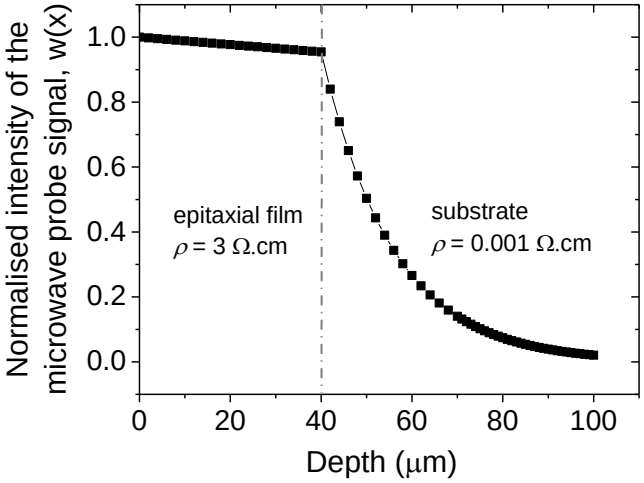

Figure 5. 12 Plot of the normalised intensity of a 10.315 GHz microwave probe signal penetrating a p/p⁺ structure where the p-type epitaxial film is 3 Ω.cm and the heavily-doped p⁺ substrate is 0.001 Ω.cm.

5.2.3.3 Decoupling bulk and surface components of effective lifetime

The asymptotic effective lifetime extracted from such μ-PCD measurements contain information about both bulk and surface/interface recombination pathways. Buczkowski *et al.* proposed a method to decouple the bulk and surface lifetimes in bulk wafers by measuring effective lifetimes using μ-PCD at two different wavelengths [57]. The resulting decay curves are distanced from each other by a function which is dependent on the sum of the surface recombination velocities. Thus, the surface and bulk lifetimes can be decoupled.

Another algorithm presented by the same authors proposes the use of a single wavelength measurement to decouple the surface and bulk contributions to the effective lifetime, by considering the strong initial decay and the asymptotic decay at the tail of the transient [58]. The strong initial decay in the case of bulk wafers contains mainly information of the surface recombination velocity. In this way, the two contributions can be distinguished. This is however not applicable for epitaxial samples with p/p⁺ structure because the initial part of the decay could not be measured reliably in experiment.

In this work, in order to separate the bulk lifetime of the epitaxial film from the sum of surface and interface recombination velocities, a variation in the thickness of the epitaxial film is introduced and multiple wafers are used to extract the bulk and surface lifetimes assuming that the bulk lifetime and surface/interface recombination velocities are identical across the different samples. This is the same approach followed by Walter and co-workers [5].

As alluded to earlier, extracting the effective lifetime from the tail of the decay transients gives the fundamental mode of decay, after all the higher order surface decay modes have died out. This effective lifetime is given by eqn. (5.15), when $S_{int} \leq 10^4$ cm/s. Thus, by measuring effective lifetimes of samples with different epitaxial layer thicknesses and performing linear fits on τ_{eff}^{-1} versus d_{epi}^{-1} plots, the bulk lifetime can be obtained from the reciprocal of the intercept with τ_{eff}^{-1}-axis while the sum of the effective surface and effective interface recombination velocities can be extracted from the gradient of the fit.

This method of extraction is illustrated in Figure 5. 13, which shows τ_{eff}^{-1} versus d_{epi}^{-1} plots calculated using eqn. (5.4)-(5.6) for different sets of bulk lifetime (10 or 100 µs) and interface recombination velocity (10^2 or 10^3 cm/s) assuming a front surface recombination velocity of 10^2 cm/s. If these effective lifetimes were to be measured in experiment instead of being calculated, one may expect an uncertainty of up to ~1-5%, depending on the averaging that is done during the measurement. This uncertainty is depicted in Figure 5. 13 using error bars.

The extracted bulk lifetimes and total effective surface/interface recombination velocities for each of the 4 cases are tabulated in Table 5. 3 in rows 1, 2, 5 and 6. The effect of different measurement uncertainties on the reliability of the extraction of bulk lifetime and total effective surface/interface recombination velocity is also illustrated in Table 5. 3. The linear fits are very good for all 4 cases, as can be seen from Figure 5. 13 and from the R^2 values in Table 5. 3. Therefore, the sum of effective surface/interface recombination velocities can be very reliably extracted from such plots, provided eqn. (5.13) is satisfied. By observing the S_{tot}^* values in Table 5. 3, it can be seen that eqn. (5.13) is satisfied for $S_{int} \leq 10^4$ cm/s.

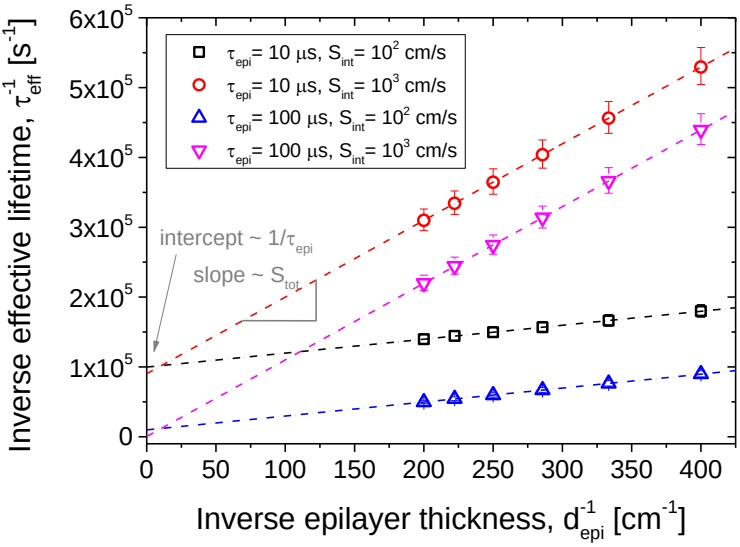

Figure 5. 13 Inverse effective lifetime calculated using eqn. (5.4)-(5.6) is plotted against inverse epitaxial layer thickness. Linear fit lines based on eqn. (5.15) are used to illustrate the extraction of bulk lifetime and sum of surface and interface recombination velocities from the intercept and slope of the fits respectively. Error bars indicate 5% uncertainty.

However, the situation is very different for the extraction of bulk lifetime. From Figure 5. 13, it can be seen that for the case of high bulk lifetime (100 µs), the intercept of the linear fits with the τ_{eff}^{-1}-axis is very close to zero. Since this axis depicts reciprocal values, the closer the intercept is to zero, the larger the uncertainty in the extraction of the bulk lifetime. In fact, even for relatively low bulk lifetimes, the uncertainty in the extraction of the bulk lifetime using this method can be high if the surface and/or interface recombination predominates as the main recombination pathway.

Table 5. 3 shows that for $S_{int} > 10^3$ cm/s, the extraction of bulk lifetime is rather unreliable especially when the bulk lifetime is high (>100 µs), leading to either negative intercepts or unreasonably high uncertainties (e.g. row 6 in Table 5. 3). For very large S_{int}, the measured effective lifetime can be equated directly to surface lifetime, since no meaningful information about bulk lifetime can be derived from fitting. Thus, in order to decouple bulk lifetime and sum of effective surface and interface recombination velocities, one term may not overwhelm the other recombination pathway, such that the effective lifetime contains sufficient extractable information about both despite the inherent measurement uncertainties. This can be done by comparing the surface lifetime with the bulk lifetime as tabulated in Table 5. 3. From this exercise, we can derive a criteria for the reliable extraction of bulk lifetime. In order that the effective lifetime contains extractable information about the bulk lifetime,

$$\tau_s > 0.1\ \tau_{epi} \tag{5.43}$$

In other words, the surface lifetime must not be less than 10% of the bulk lifetime, for the measurement uncertainties of ~1-5% that are typical of µ-PCD measurements reported in this thesis, in order to be able to extract τ_{epi} reliably.

Besides measurement uncertainties, there will be additional variations due to within-wafer non-uniformities, wafer-to-wafer process variations during epitaxial growth or during passivation, as well as errors in the effective lifetime extraction process.

Table 5. 3 Bulk lifetimes and the sum of effective surface/interface recombination velocities extracted from linear fits such as those in Figure 5. 13, together with the standard errors (abbreviated as "std. error") assuming 0%, 2% and 5% measurement uncertainties. Such linear fits were done for different combinations of τ_{epi} and S_{int}. The R^2 values for the fits are also given. It can be seen that if condition (5.13) is not satisfied, extraction of S_{int} becomes unreliable and if condition (5.43) is not met, then extraction of τ_{epi} becomes unreliable.

No.	Assumed for calculation				Extraction based on linear fits to eqn. (5.15)								
	τ_{epi}	S_{int}	S^*_{tot}	τ_s	τ_{epi}	Std. error (0%)	Std. error (2%)	Std. error (5%)	S_{tot}	Std. error (0%)	Std. error (2%)	Std. error (5%)	R^2
1	10	10^2	0.03	20.1	10.0	0.019	0.555	1.43	199.8	0.684	19.9	51.2	0.99994
2	10	10^3	0.15	3.78	11.1	0.026	1.71	4.42	1098	0.806	52.6	136	1.00000
3	10	10^4	1.41	0.59	-2.00	-	-	-	9239	68.1	284	732	0.99973
4	10	10^5	14.0	0.26	-0.273	-	-	-	31180	1370	708	1830	0.9904
5	100	10^2	0.03	20.1	102	2.02	23.0	55.9	199.7	0.739	8.39	20.4	0.99993
6	100	10^3	0.15	3.78	2630	1.51×10^3	7.12×10^4	1.73×10^5	1097	0.837	39.6	96.2	1.00000
7	100	10^4	1.41	0.59	-1.70	-	-	-	9236	68.5	261	635	0.99973
8	100	10^5	14.0	0.26	-0.267	-	-	-	31140	1370	668	1620	0.99036
9	250	10^2	0.03	20.1	262	13.5	139	335	199.7	0.749	7.67	18.6	0.99993
10	250	10^3	0.15	3.78	-178	-	-	-	1097	0.840	38.9	94.4	1.00000
11	250	10^4	1.41	0.59	-1.68	-	-	-	9235	68.5	261	633	0.99972
12	250	10^5	14.0	0.26	-0.267	-	-	-	31140	1370	667	1620	0.99036

5.3 Lifetime measurements on epitaxial films detached from the parent substrate

As explained in Chapter 1, in LT-epicells, porous silicon enables the detachment of an epitaxial layer from the substrate. Detaching the epitaxial film from the parent substrate significantly simplifies the evaluation of the minority carrier lifetime in the epitaxial film, since the influence of the parent substrate on the measurement of lifetime is eliminated. This allows a host of standard lifetime measurement techniques, used in photovoltaic research for wafer-based silicon, to be used for evaluating epitaxial foils, including quasi-steady state photoconductance (QSSPC) [3], which is the most-commonly used lifetime measurement method.

For evaluation of the minority carrier lifetime of epitaxial foils, QSSPC has been used throughout this thesis. Figure 5. 14 shows the schematic drawing of a passivated epitaxial foil without the residual porous silicon used in QSSPC measurements. Compared to sim-PL which is a purely steady-state method and μ-PCD which is a purely transient method, QSSPC is somewhere in between and combines the advantages of both steady-state and transient methods. In particular, with QSSPC, it is possible to evaluate the minority carrier lifetimes across several orders of magnitude in injection level, thus yielding injection level-dependent effective lifetime curves.

In this technique, a laser (800 nm wavelength) is used to irradiate the sample (see Figure 5. 14), which creates excess carriers in silicon. During the measurement, the laser intensity is continuously and slowly reduced over several orders of magnitude. This results in a concomitant reduction in the excess carrier concentration in the sample. However, the characteristic decay time of the laser intensity is kept larger or comparable to the effective lifetime of the sample so that the minority carrier concentration in the sample appears to be in steady-state at each instantaneous time during the decay of the laser intensity. The carrier density in a semiconductor sample is related to its conductance. So, as the average excess carrier density, Δn_{av} in the sample changes, the excess photo-conductance also changes as follows

$$\Delta n_{av} = \frac{\Delta\sigma(t)}{q(\mu_n + \mu_p)d_{epi}} \tag{5.44}$$

During a QSSPC measurement, the sample is inductively coupled by a coil to a radio-frequency bridge which measures the changes in the conductance The average excess carrier density of the sample can then be extracted.

Starting from the continuity equation for minority carriers in such a system, Nagel *et al.* derived a generalised analysis procedure to interpret the results of QSSPC measurements [59], resulting in the following general expression of the effective lifetime

$$\tau_{eff} = \frac{\Delta n_{av}}{G_{av}(t) - \frac{\partial \Delta n_{av}(t)}{\partial t}} \tag{5.45}$$

where

$$G_{av}(t) = \frac{\phi_0 f_{abs}}{d_{epi}} \tag{5.46}$$

The average generation rate, G_{av}, in the sample is determined from the flux density of the illumination, ϕ_0, that is measured by an external detector and the absorption fraction, f_{abs}, that is evaluated based on the total external reflectance of the sample.

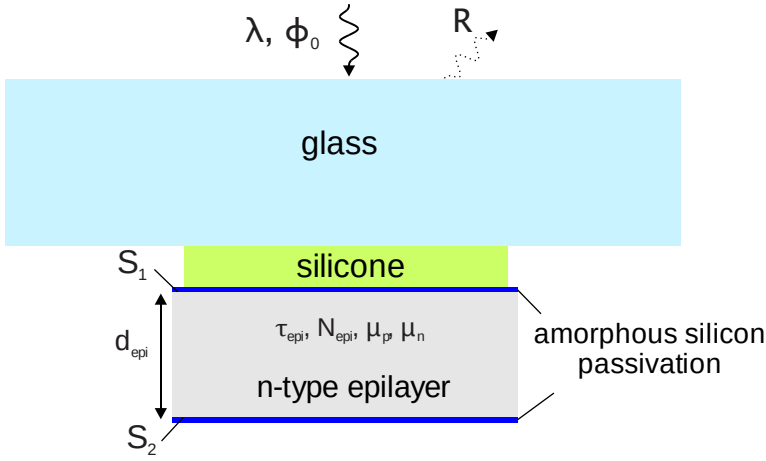

Figure 5. 14 Schematic of the cross-section of a passivated epitaxial foil bonded to glass using silicone. A hydrogenated 10 nm thick intrinsic amorphous silicon and 20 nm thick n^+-doped amorphous silicon stack is for passivation of both surfaces (whose surface recombination velocities are denoted as S_1 and S_2).

From the effective lifetime measured using QSSPC, it is possible to extract the bulk lifetime using a similar method outlined in Section 5.2.3.3 for μ-PCD measurements (see Figure 5. 13 for example). This would require several samples with different epitaxial layer thicknesses to be used. However, this is not widely used in the work of this thesis because the typical detachment yield of epitaxial foils is rather low: ~50-60%. This also varies significantly from run to run with some experimental runs resulting in as low as 0% detachment yield. So, a large amount of redundancy per thickness point is required. Thus, a different method is followed to extract the bulk lifetime.

The total effective surface recombination velocities ($S_{tot} = S_1 + S_2$) are obtained using reference Float Zone (FZ) wafers which go through the same processing sequence as the epitaxial foils, with the exception of detachment. From the lifetime measurements on these reference FZ wafers, S_{tot} is obtained by assuming that the measured effective lifetime is approximately equal to the total surface lifetime i.e. the bulk lifetime is so high that it can be neglected. This is usually a very good assumption, and widely used in research. Another way in

which S_{tot} can be estimated is by using lithography-based epitaxial foils, which have nearly 100% detachment yield compared to the porous silicon-based epitaxial foils. Lithography-based epitaxial foils are explained more in detail in Chapter 6. By using lithography-based epitaxial foils of different thicknesses, both the bulk lifetime, τ_{epi}, and the total effective surface recombination velocity, S_{tot}, can be obtained. These lithography-based epitaxial foils also act as reference for the porous silicon-based epitaxial foils.

Thus, the bulk lifetime of porous silicon-based epitaxial foils can be obtained using the following expression

$$\tau_{epi} = \tau_{eff} - \frac{S_{tot}}{d_{epi}} \tag{5.47}$$

where τ_{eff} is measured using QSSPC of the porous silicon-based epitaxial foils and S_{tot} is obtained from the reference FZ wafers or lithography-based epitaxial foils.

However, since the residual porous silicon is removed after detachment and before passivation of the rear side, we can expect rather low surface recombination velocities for both surfaces. Thus, the measured effective lifetime in itself is a very good indicator of the quality of the epitaxial foil and is predominantly used as the figure of merit.

A final note is made here about the reference used for comparison of lifetime measurements on detached epitaxial foils. While epitaxial growth on pristine p^+ silicon acts as a reference layer for the attached epitaxial layers, for the detached epitaxial foils, the lithography-based foils act as reference foils, which will be described more in detail in Chapter 6.

5.4 Chapter summary

- Porous silicon can influence the effective minority carrier lifetime of epitaxial layers, when attached to a p^+ silicon substrate and detached from it, in several ways.
- The surface topography and intrinsic stress distribution of porous silicon and its metal gettering efficiency would influence the bulk lifetime of the epitaxial layer. In attached epitaxial layers, porous silicon would also exacerbate the interface recombination at the p/p^+ junction. In detachable epitaxial foils, the ease of detachment can also affect the quality of the detached epitaxial foil.
- Measuring lifetime in attached epitaxial layers is challenging because the p^+ silicon substrate restricts the range of applicable lifetime measurement techniques and the high interface recombination makes it difficult to extract the bulk lifetime.
- In detached epitaxial foils, handling of fragile free-standing epitaxial foils is difficult due to easy breakage. On the other hand, when they are handled in

a glass-bonded configuration, the presence of silicone complicates the wet chemical treatment and passivation steps.

- For attached epitaxial layers, two lifetime measurement methods were presented, namely simulation-assisted photoluminescence (sim-PL) and microwave-detected photoconductance decay (μ-PCD).
- Simulation-assisted photoluminescence (sim-PL):
  - With sim-PL, the bulk lifetime, τ_{epi}, and the effective interface recombination velocity, S_{int}, are extracted directly by calculating the ratio of PL intensities from epitaxial layers of two different thickness and relating it to (τ_{epi}, S_{int}) solution sets via numerical modeling (eqn. (5.19)).
  - The PL from the substrate is shown to contribute significantly to the total measured PL signal (Figure 5. 7) in the absence of porous silicon. This contribution must be corrected before extraction of τ_{epi} and S_{int}.
  - Analytical modeling of the excess carrier densities in the substrate is performed in order to derive an elegant expression for the correction of PL signal from the substrate (eqn. (5.39)) when the substrate excess carrier density is injection-dominated. On the other hand, when the excess carrier density is dominated by photo-generation, a correction can be made by measuring PL directly on the substrate and multiplying it with a factor of $e^{-\alpha d_{epi}}$ to account for the absorption in the epitaxial layer.
  - On the other hand, the substrate PL is suppressed when an embedded porous silicon layer is present at the interface.
  - This technique is not applicable for very low lifetime epitaxial layers. Moreover, it is insensitive to $S_{int} < 10^3$ cm/s and only ballpark values for S_{int} can be obtained.
- Microwave-detected photoconductance decay (μ-PCD):
  - The effective lifetime of the epitaxial layer can be measured directly using μ-PCD.
  - The influence of the substrate on the measurement is minimal because firstly, the microwave probe signal is several attenuated in the substrate and secondly, the sensitivity of the μ-PCD tool in high conductivity silicon is negligible.
  - To extract τ_{epi} and the sum of the effective surface and effective interface recombination velocity, S_{tot}, effective lifetime is measured on several epitaxial layer samples with different thicknesses. From a plot of $1/\tau_{epi}$ versus $1/d_{epi}$, τ_{epi} is obtained from the reciprocal of $1/\tau_{epi}$-axis intercept and S_{tot} from the slope.
  - This technique is very sensitive for extraction of S_{tot}. However, when the interface recombination dominates the bulk recombination, reliable information about τ_{epi} cannot be obtained.

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Chapter 6
Lifetime measurements in epitaxial layers: Experimental studies

In this chapter, minority carrier lifetime measurements performed on epitaxial layers attached to p^+ silicon substrate as well as detached epitaxial foils are presented and interpreted. Appropriate reference layers are used in each case to compare with epitaxial layers grown on annealed porous silicon.

6.1 Lifetime measurements on attached epitaxial layers

6.1.1 Sample preparation and characterisation details

Samples for lifetime measurements were prepared starting from mirror-polished, 200 mm diameter, Czochralski-grown (Cz), p^+ silicon substrates with a boron doping concentration of $1\text{-}2\times10^{19}$ cm^{-3}. After surface cleaning, a layer of porous silicon with an average porosity of ~28% and a typical thickness of ~400 nm is etched onto the front surface of such substrates. The area of porous silicon is ~8.5 cm by 8.5 cm in the middle of the wafer of 200 mm diameter. Therefore, it is possible to measure lifetime of epitaxial p/p^+ structures with and without porous silicon on the same wafer.

The porous silicon etching process is followed by a high temperature bake at 1130 ^oC for 10 min in hydrogen (H_2) ambient at atmospheric pressure, during which the as-etched columnar pores coalesce into large enclosed voids, resulting in a closed and smooth top surface amenable for high quality epitaxial growth. Subsequently, an in-situ epitaxial chemical vapour deposition (CVD) of silicon is carried out using trichlorosilane (TCS) at the same temperature and pressure. For lifetime measurements on attached epitaxial layers, only p-type epitaxial films with boron doping concentration of $\sim10^{16}$ cm^{-3} were grown with thickness ranging

from 20-50 µm. In some samples, a 1-2 µm thick BSF (with a boron doping concentration of $1\text{-}2\times10^{19}$ cm^{-3}) is grown epitaxially at the interface with the substrate.

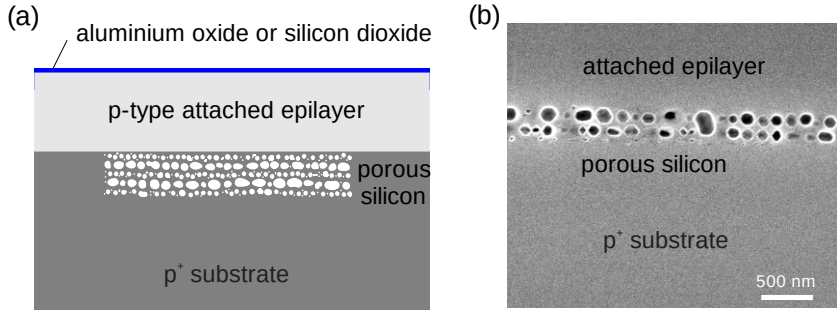

Figure 6. 1 (a) Schematic diagram (not drawn to scale) depicting the cross-sectional view of a lifetime sample where an epilayer (20-50 µm thick), grown on top of an embedded porous silicon layer, remains attached to a p^+ substrate. The front surface is passivated with aluminium oxide; (b) a cross-sectional scanning electron microscopy (XSEM) image showing the microstructure of the porous silicon corresponding to (a).

The front surface is passivated with either aluminium oxide or silicon dioxide. Aluminium oxide is deposited using atomic layer deposition (ALD) at 200°C, followed by a forming gas anneal (FGA) at 400°C. Silicon dioxide is grown using dry thermal oxidation at 1050 °C. The cross-sectional schematic and scanning electron microscopy (SEM) image of a typical sample are shown in Figure 6. 1. The quality of epitaxial layers grown in this way are evaluated by lifetime measurements using the two techniques described in Chapter 5: simulation-assisted steady-state photoluminescence (sim-PL) and microwave-detected photoconductance decay (µ-PCD).

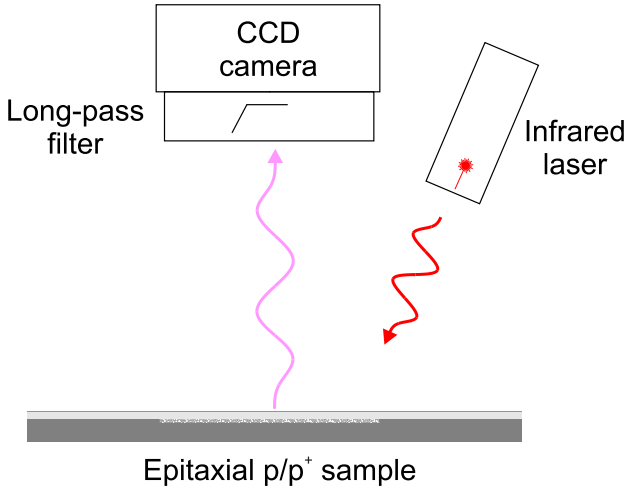

Figure 6. 2 A schematic diagram of the photoluminescence measurement set-up used for the sim-PL method.

For sim-PL, the LIS-R1 PL imaging tool from BT Imaging (Surry Hills, NSW, Australia) is used, also in a front-front configuration. The set-up is schematically depicted in Figure 6. 2. The sample is irradiated with a 808 nm laser at a constant photon flux of 2.5×10^{17} /cm^2. A silicon charge-coupled device (CCD) camera fitted with a standard lens is use to image the PL signal emitted by the sample with a lateral resolution of 160 µm. A long pass optical filter (Schott glass RG1000) is used to block all photons with wavelength below 1000 nm so that the reflected light from the incident laser does not affect the PL image. The integration time is ~1-2 s.

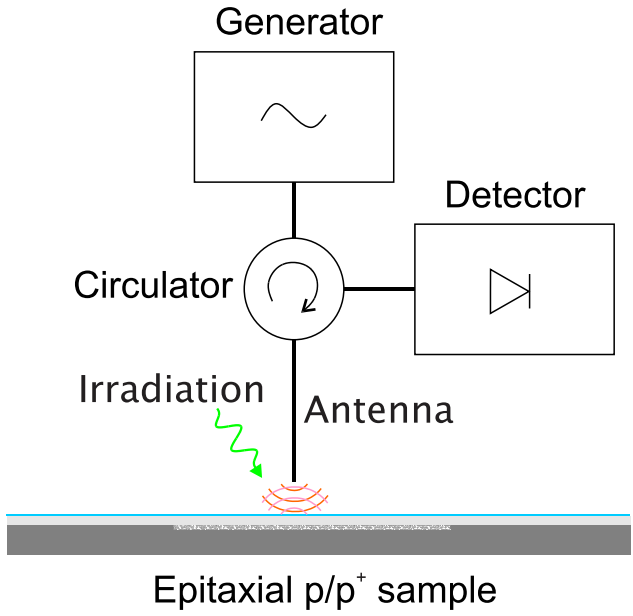

Figure 6. 3 Diagram depicting a µ-PCD measurement set-up, depicting the microwave generator, circulator and detector. A antenna used for probing and detection is in non-contact mode with a diameter of 400 µm. The excitation area of 1 mm².

For µ-PCD, the WT-2000 Multifunctional Wafer Mapping Tool from Semilab Co. Ltd. (Budapest, Hungary) was used in a front-front configuration. This is schematically depicted in Figure 6. 3. The sample is irradiated with monochromatic light with a wavelength of 904 nm or 532 nm with an intensity of ~1-3×10^{13} photons per pulse. As discussed in Chapter 5, due to the skin depth of the microwave probe signal and the poor sensitivity towards conductivity changes in the heavily-doped substrate, both wavelengths are viable to be used for measurements of epitaxial layer structures for the thickness range used in this thesis. The excited area is about 1 mm^2, while the diameter of the microwave antenna head is about 400 µm. Microwaves are generated at a frequency of ~10.3 GHz, adjusted to maximise sensitivity and minimise non-linearity. The circulator directs the microwaves from the generator on the sample surface and the reflected microwaves on to the detector. Changes in the reflectivity corresponding to changes in the conductivity of the epitaxial layer are measured by the detector as

changes in voltage. The recorded decay transient is fitted with a mono-exponential relation with data from the tail part of the decay to calculate the effective lifetime of the epitaxial layer. Between 256 and 1024 such measurements are made at each spot and an average is taken for the effective lifetime of each spot. This reduces the uncertainties associated with the measurement and extraction procedure to <2%. The raster size is varied between 0.5 and 2 mm^2, which determines the resolution of the resulting effective lifetime map.

6.1.2 Experimental results and discussion

As mentioned before, in order to understand the influence of porous silicon on the bulk lifetime of the epitaxial layer that is grown on top and the effective interface recombination velocity at the interface between the epitaxial layer and the substrate, the various parameters listed in Table 5.2 in Chapter 5 must be evaluated. This is because the epitaxial film grown on pristine silicon stands as the reference for the epitaxial films grown on annealed porous silicon.

In the first experimental run, epitaxial p/p^+ samples with three different thicknesses, namely 20, 30 and 40 μm, were prepared, as described in Section 6.1.1. Two sets of samples were prepared: one set had a 2 μm-thick BSF shielding the epitaxial layer / p^+ substrate interface and the other set not. These samples were passivated with aluminium oxide on the front side.

The technique of sim-PL will be explored first to study these epitaxial p/p^+ samples. Steady-state PL measurements result in uncalibrated maps such as the one shown in Figure 6. 4, for the case of a 40 μm thick p-type epitaxial layer with a p^+ silicon BSF shielding the interface between the epitaxial layer and the p^+ substrate. The square-like pattern of ~8.5 cm by 8.5 cm in the middle of the map corresponds to an epitaxial layer that is grown on embedded porous silicon, while the peripheral area is associated with an epilayer grown on pristine silicon.

From such maps, representative areas of 200 by 200 pixels in size (also indicated in Figure 6. 4) without local non-uniformities or abnormalities are chosen to calculate the average PL intensity both in the regions with and without porous silicon (on the same wafer). For the region with porous silicon, the representative area is chosen such that it is also away from the edge where the quality of the epilayer is evidently poor, as can be observed from the dark line delineating the central porous region. This dark line in fact corresponds to the region where the wafer surface makes contact with an O-ring during porous silicon etching, leading to lower quality epitaxy.

Figure 6. 5 shows the average PL intensity as a function of epitaxial layer thickness. It is observed that the PL intensity increases as epitaxial layer thickness increases for all four configurations. This means that the epitaxial layer is not in the low bulk lifetime regime (see Figure 5.6 in Chapter 5), where this method would fail.

The PL intensity in the area with embedded porous silicon is in general lower (see Figure 6. 4 and Figure 6. 5 (b)) than that in the peripheral areas without porous silicon. This can due to two reasons: (1) the excess carrier density level of

the epitaxial layer in the porous silicon area is lower compared to that in the area without porous silicon and/or (2) the substrate contribution to the measured PL signal is lower in the porous silicon area.

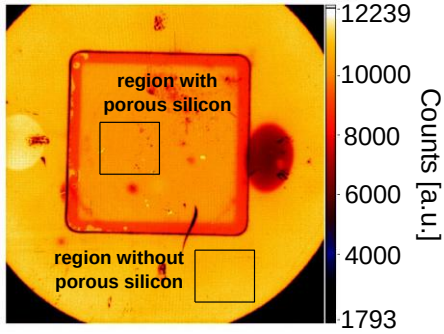

Figure 6. 4 An uncalibrated photoluminescence map of an aluminium oxide-passivated p-type (10^{16} cm^{-3} boron concentration) epitaxial layer grown on a p^+ (10^{19} cm^{-3} boron concentration) silicon substrate, shielded by an epitaxially-grown BSF (10^{16} cm^{-3} boron concentration). The square-like area of ~8.5 cm by 8.5 cm in the middle has embedded porous silicon.

Substrate contribution is illustrated in Figure 6. 5 by making use of linear fit lines to connect the data points. From the modelling work of Chapter 5, Section 5.2.2, it was seen that a plot of PL intensity versus epitaxial layer thickness would be approximately linear if the epitaxial layer bulk lifetime is high (≥ 50 µs) for the typical barrier ratios (N_{epi}/N_{sub} = 10^{16} / 1-2×10^{19} cm^{-3}) used in this thesis. However, it should be noted that a linear fit has no physical meaning and is simply a guide to the eye to illustrate where such a fit line would intersect the PL intensity-axis. A large non-zero intercept for linear fit lines to measurements on a high lifetime epitaxial layers would mean a significant part of the measured PL intensity comes from the substrate underneath the epitaxial layer. However, it should be noted that in samples with low lifetime epitaxial layers (≤ 10 µs) and/or low barrier ratios, the PL intensity versus epitaxial layer thickness can be highly non-linear. Thus, a good linear fit also indicates bulk lifetimes > 50 µs, even before extraction.

For measurements in the area without porous silicon (Figure 6. 5 (a)), it is clear that that a simple linear fit to the data points leads to a significant non-zero intercept. Thus, the measured PL intensities must be corrected in these cases. In order to correct this total PL intensity, the PL contribution from the substrate, calculated based on eqn. (5.39) proposed in Chapter 5, Section 5.2.2.2, is subtracted. The doping concentration obtained from SIMS measurements is ~1.5×10^{19} cm^{-3}. The resulting corrected PL intensities are also plotted in Figure 6. 5 (a). Linear fits to the corrected data points intersect the axes close to the origin.

In contrast, as illustrated in Figure 6. 5 (b), for the PL intensities measured in the area with porous silicon, linear fits intersect close to the origin. This indicates that the substrate PL contribution to the measured PL intensity in the porous silicon area is suppressed, as was also expected from the discussion in Chapter 5, Section 5.2.2.2.

Moreover, from Figure 6. 5 (b), it can be observed that in samples without a BSF, the PL intensity in the porous silicon is extremely low, indicating that the excess carrier density level and the effective lifetime of the epitaxial layer is certainly reduced by the enhanced interface recombination when there is no BSF present. However, to know if the epilayer bulk quality is detrimentally affected by the porous silicon or not, the bulk lifetime needs to be evaluated.

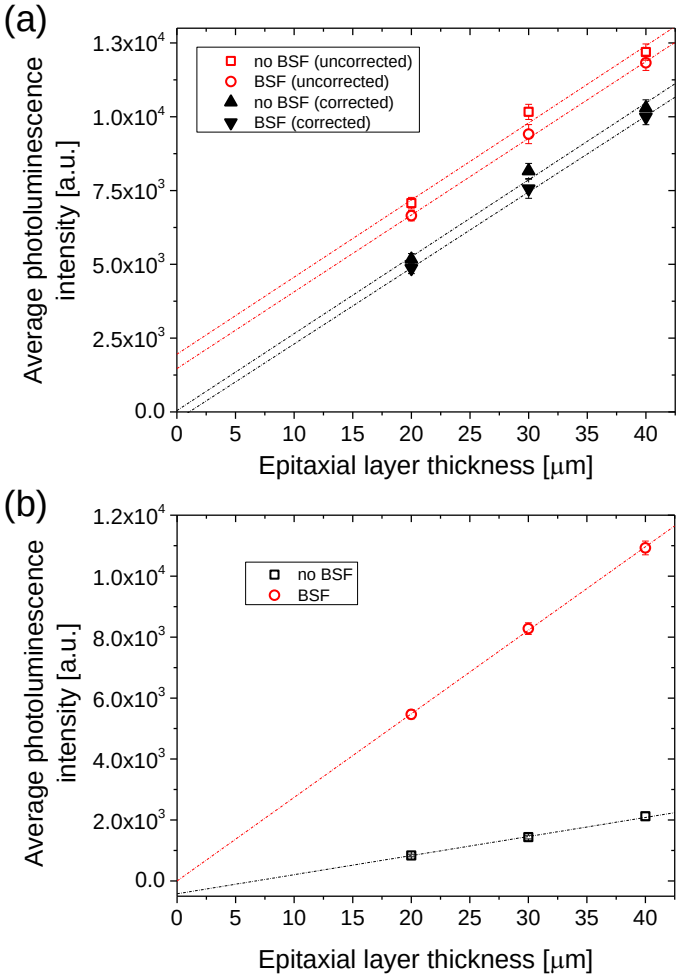

Figure 6. 5 Average PL intensity as a function of the epitaxial layer thickness for (a) epitaxial layers grown on pristine silicon and (b) annealed porous silicon, in samples with and without a BSF. Linear fit lines have been added as a guide to the eye. The substrate PL intensities, calculated based on eqn. (5.39), are subtracted from the measured PL intensities to yield the corrected plots in (a). For measurements in the porous silicon area, such corrections were deemed unnecessary.

At first, the bulk lifetimes of epitaxial layers grown on pristine silicon were extracted. Ratios of PL intensities were calculated based on the corrected PL

intensities. Two combinations of thicknesses yielding large PL ratios were chosen, namely the 40 µm-20 µm pair and the 30 µm-20 µm pair. For each thickness pair, a set of calibration curves for three different S_{int} values of 10^2, 10^3 and 10^4 cm/s were calculated from numerical simulations based on PC1D, as shown in Figure 6. 6. The experimentally-obtained PL ratios are plotted as horizontal lines intersecting the calibration curves, from which $\tau_{epi,no\ PS}$ values have been read off from the horizontal axis (shown in Figure 6. 6 for $R_{40\mu m/20\mu m}$). All extracted results are summarised in Table 6. 1.

Since there is a calibration curve corresponding to each S_{int}, a different τ_{epi} value is extracted for each curve, resulting in a set of solutions (τ_{epi}, S_{int}), of which the correct solution must be selected. In Figure 6. 6, the calibration curves corresponding to $S_{int} = 10^2$ or 10^3 cm/s more or less coincide. Thus, the extracted τ_{epi} values would be similar. For example, for the epitaxial layers with a BSF, the extracted bulk lifetime values are 135 µs and 110 µs respectively, while for those without a BSF, the extracted bulk lifetimes are 95 µs and 80 µs respectively.

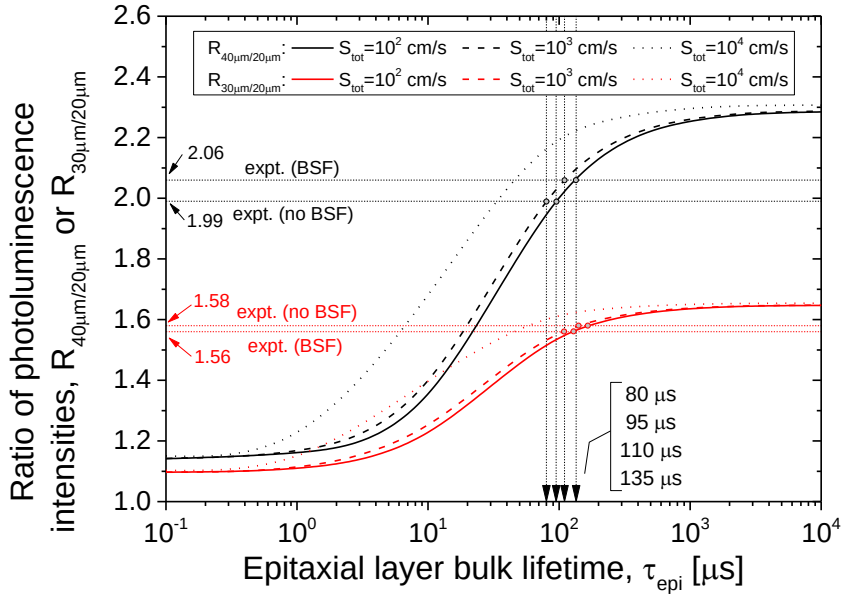

Figure 6. 6 Calibration chart showing two sets of curves corresponding to two thickness pairs for various S_{int} (10^2, 10^3 and 10^4 cm/s).

Moreover, irrespective of whether the $R_{40\mu m/20\mu m}$ curves or the $R_{30\mu m/20\mu m}$ curves are used in the extraction, the extracted τ_{epi} values are similar (110-135 µs using $R_{40\mu m/20\mu m}$ curves compared to 110-130 µs for the $R_{30\mu m/20\mu m}$ curves for the epitaxial layers with a BSF), illustrating the robustness of this method. Note that for the epitaxial layers without a BSF, the spread in the extracted lifetimes is wider because of an anomalously higher PL intensity measured for the 30 µm thick epitaxial layer or equivalently a lower PL intensity measured for the 40 µm thick epitaxial layer (see Figure 6. 5 (a)).

On the other hand, the τ_{epi} values extracted if we assume $S_{int} = 10^4$ cm/s are considerably lower (35-55 µs). In order to arrive at the correct solution set, an additional constraint must be used. This comes in the form of a µ-PCD measurement on the BSF-shielded 30 µm-thick epitaxial layer sample, which resulted in τ_{eff} values in the range of 2.1-2.4 µs outside the porous silicon area. Table 6. 1 also gives effective lifetime values calculated for each (τ_{epi}, S_{int}) solution set, based on eqn. (5.15). When comparing these calculated τ_{eff} values with the τ_{eff} values measured using µ-PCD, we can conclude that indeed S_{int} is in the range of 10^3 cm/s and the corresponding bulk lifetimes extracted from Figure 6. 6 are in the range of 80-110 µs. As expected, the back surface field appears to have no effect in improving S_{int} in the case when the epilayers on grown on pristine silicon.

Table 6. 1 Epitaxial layer bulk lifetimes extracted using two sets of calibration curves based on two thickness pairs for samples with epitaxial layers grown on pristine p⁺ silicon substrate with and without BSF. In each set, three calibration curves corresponding to three different effective interface recombination velocities were used. The last two columns show the calculated effective lifetimes based on eqn. (5.15).

Pair	Extracted from sim-PL			Calculated using eqn. (5.15)	
	S_{int} [cm/s]	$\tau_{epi,no\ PS}$ (no BSF) [µs]	$\tau_{epi,no\ PS}$ (BSF) [µs]	τ_{eff} (no BSF) [µs]	τ_{eff} (BSF) [µs]
$R_{40\mu m/20\mu m}$	10^2	95	135	23	25
	10^3	80	110	2.9	2.9
	10^4	35	45	0.30	0.30
$R_{30\mu m/20\mu m}$	10^2	165	130	25	24
	10^3	140	110	2.9	2.9
	10^4	55	45	0.30	0.30

It should be noted that one of the disadvantages of sim-PL is that it is not possible to specify a precise value for S_{int}, but only ballpark numbers, since a choice must be made among a discrete set of solutions. Another note-worthy point is that even though µ-PCD measurement is used as a way to impose an additional constraint on a family of solutions, strictly-speaking, it is not accurate to compare the effective lifetimes from µ-PCD measurements with the ones which are calculated from the extracted values based on sim-PL because µ-PCD is a transient technique which measures effective lifetime at a much higher injection level compared to sim-PL. However, since we are dealing with ballpark values for S_{int} which differ by an order of magnitude to the next one, it is still reasonable to use this approach.

Similarly, for the measurements in the porous silicon area, we can use the same approach outlined above. For instance, µ-PCD measurements on the same sample (30 µm thick BSF-shielded epitaxial layer) inside the porous silicon area resulted in effective lifetimes in the range of 1.6-2.0 µs. From these measurements and similar calculations as given in Table 6. 1, we can gauge that the ballpark number for the S_{int} of a BSF-protected epitaxial layer with an embedded porous silicon is again ~10^3 cm/s.

A second method in which we can derive the ballpark value of S_{int} of a BSF-protected epitaxial layer with an embedded porous silicon layer is to consider the ratio of PL signals from areas with and without porous silicon but on the same wafer (same d_{epi}). Similar to eqn. (5.19) in Chapter 5,

$$R_{PS/no\ PS} = \frac{I_{PL,PS}}{I_{PL,no\ PS}} = \frac{\Delta n_{av,PS}.\, d_{epi}}{\Delta n_{av,no\ PS}.\, d_{epi}} = \frac{\tau_{eff,PS}}{\tau_{eff,no\ PS}} = \frac{\frac{1}{\tau_{epi,no\ PS}} + \frac{1}{\tau_{s,no\ PS}}}{\frac{1}{\tau_{epi,PS}} + \frac{1}{\tau_{s,PS}}} \tag{6.1}$$

where τ_s is given by eqn. (5.5) in Chapter 5. The values of $\tau_{epi,no\ PS}$ and $\tau_{s,no\ PS}$ are known from the discussion above. Assuming a value of 100 µs for $\tau_{epi,no\ PS}$ and 10^3 cm/s for $S_{int,no\ PS}$, the ratio $R_{PS/no\ PS}$ is plotted for different $S_{int,PS}$ and $\tau_{epi,PS}$ values in Figure 6. 7. The experimentally-obtained ratios from samples with BSF are approximately 1 for all thicknesses, which is indicated as a horizontal dotted red line in Figure 6. 7. Let us assume that $S_{int,PS/BSF} \geq S_{int,no\ PS/BSF}$. This would mean that in order for the experimental ratios to intersect one of the curves, the bulk lifetime of epilayers on top of porous silicon, $\tau_{epi,PS}$ should be ≥ 50 µs. Intersection of the experimental ratios with any of the curves associated with $\tau_{epi,PS} \geq 50$ µs results in $S_{int,PS/BSF}$ in the range of $\sim 10^3$ cm/s. This is a significant result because it implies that a 2 µm-thick epitaxially-grown BSF completely shields the porous silicon i.e. the BSF makes the porous silicon completely electronically "opaque" to minority carriers in the epitaxial layer.

Since all of the reduced set of curves (for $\tau_{epi,PS} \geq 50$ µs) in Figure 6. 7 intersect the experimental line at around the same $S_{int,PS}$ value, we can therefore ignore the first term associated with τ_{epi} in the denominator and the numerator of eqn. (6.1) to arrive at an approximation

$$R_{PS/no\ PS} \approx \frac{\tau_{s,PS}}{\tau_{s,no\ PS}} \tag{6.2}$$

which states that the ratio of PL intensities, $R_{PS/no\ PS}$, is approximately equal to the ratio of the surface lifetimes. Moreover, since the condition (5.13) (see Chapter 5) is also satisfied for the case when the porous silicon is shielded by a BSF, we can drop the diffusion-related term of the surface lifetime. Furthermore, assuming that $S_{int,PS} \gg S_{fr}$, we can write

$$R_{PS/no\ PS} \approx \frac{S_{int,no\ PS/BSF}}{S_{int,PS/BSF}} \tag{6.3}$$

Therefore, under these assumptions, the ratio of PL signals, $R_{PS/no\ PS}$, gives the ratio between the effective interface recombination velocities in the two regions. Since the measured ratios are close to 1, we can expect the effective interface recombination in the case of BSF-shielded porous silicon to be about the same as that without porous silicon (as was seen to be the case from the earlier discussion related to Figure 6. 7). In other words, the BSF is very effective in shielding the minority carriers from the highly-recombinative porous silicon. However, this

result must be taken with a pinch of salt, since sim-PL method only gives ballpark numbers for S_{int}, and not the precise values.

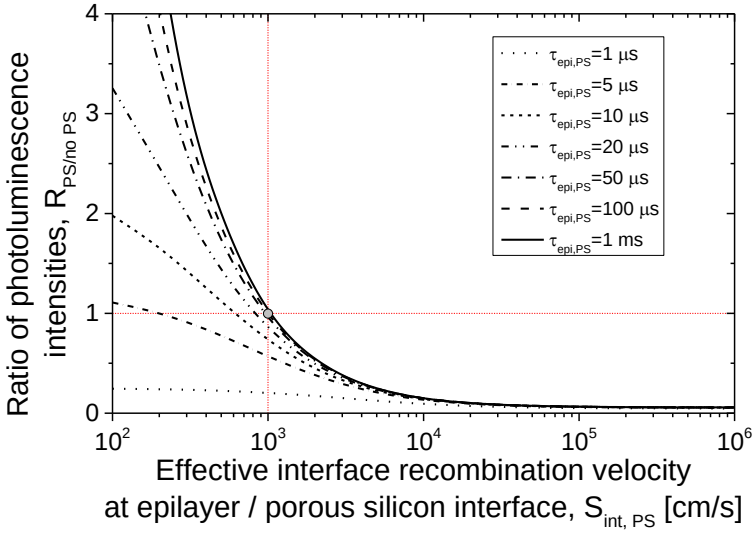

Figure 6. 7 Ratio of PL intensities from areas with and without porous on the same wafer (i.e. same epilayer thickness) for different $S_{int,PS}$ and $\tau_{epi,PS}$ values, calculated based on eqn. (6.1). $\tau_{epi,no\ PS}$ and $S_{int,no\ PS}$ are assumed to be 100 µs and 10^3 cm/s respectively.

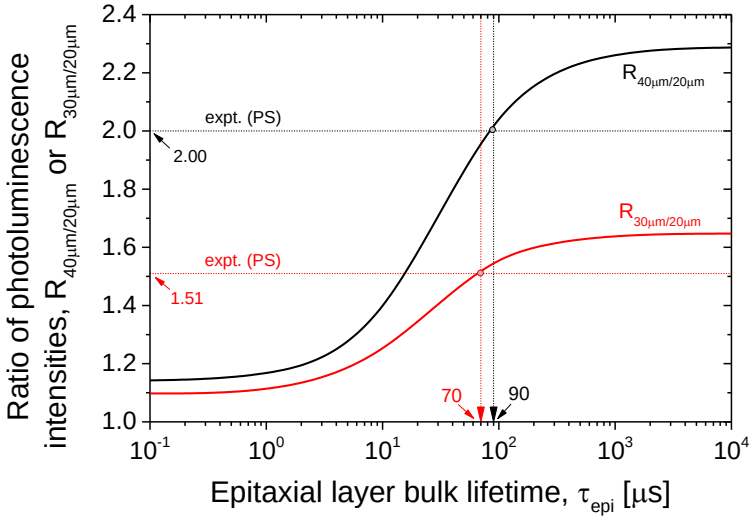

Figure 6. 8 Calibration chart showing two sets of curves corresponding to two different thickness pairs for S_{int} = 10^3 cm/s. The experimental ratios obtained from PL measurements in regions with BSF-shielded porous silicon are also plotted as horizontal lines and are shown to intersect the calibration curves.

Now that $S_{int,PS/BSF}$ is known, calibration chart of Figure 6. 8 can be used to evaluate the bulk lifetime of epilayers grown on areas with porous silicon. In Figure 6. 8, again two sets of curves corresponding to two thickness pairs have been plotted for the S_{int} value of 10^3 cm/s. The dotted horizontal lines correspond to the experimental ratios obtained from measurements in areas where a BSF protects the porous silicon. The intersections of these lines with the respective curves result in $\tau_{epi,PS}$ in the range of 70-90 µs. This is very much comparable to the $\tau_{epi,no\ PS}$ reference values of 80-110 µs extracted previously in regions without porous silicon.

A discussion on the comparison of the bulk lifetime extracted in epitaxial layers grown on annealed porous silicon with that of the reference epitaxial layers grown on pristine silicon will be deferred to the end of this section, where the results of several experiments will be compiled and discussed.

The bulk lifetime of the epilayer grown on top of porous silicon should be the same in regions with and without BSF, assuming stable processing conditions for all wafers. This is because in both cases, the epitaxial growth template, i.e. the annealed porous silicon surface, is the same. Thus, the defect density is expected to be similar. Moreover, the metal gettering effects (if any) would not be altered by the presence of a BSF. Thus, knowing $\tau_{epi,PS}$ allows us to extract the effective interface recombination velocity of the epilayer-porous silicon interface that is not protected by a BSF.

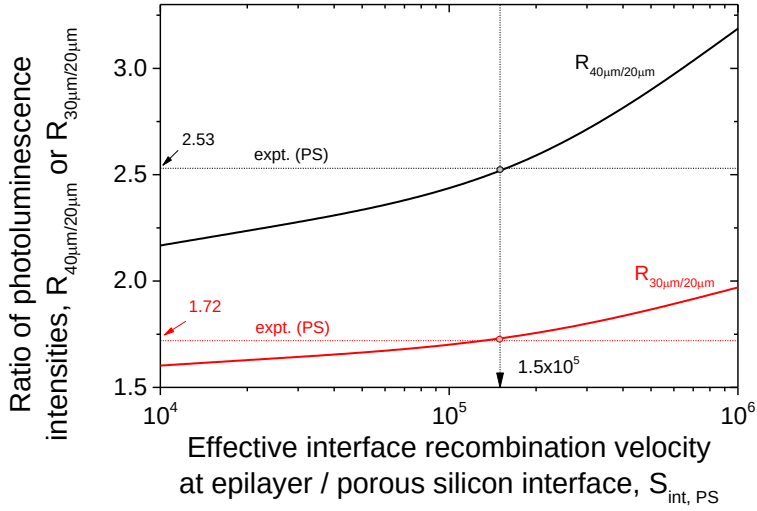

Figure 6. 9 Calibration chart with R_{d_1/d_2} plotted as a function of S_{int} for τ_{epi} =100 µs. The experimental ratios obtained from measurements on epitaxial layers grown on annealed porous silicon without a BSF are also plotted as horizontal lines and are shown to intersect the calibration curves from which $S_{int,PS}$ can be extracted.

Re-plotting the calibration chart with ratios R_{d_1/d_2} as a function of S_{int} for $\tau_{epi,PS}$ = 80 µs, we get the curves in Figure 6. 9. The experimentally-obtained ratios are also plotted as horizontal lines. Note that the experimentally-found PL

intensity ratios in this case is much higher than all the other cases. This indicates that epitaxial layers grown on annealed porous silicon without a BSF shield are in the regime of high S_{int}, where the sensitivity of the calibration curve to $S_{int}$is also high, as discussed previously (see Figure 5.6 in Chapter 5). From the intersection of the experimental lines and the simulated curves, a $S_{int,PS/no\ BSF}$ value of ~ 1.5×10^5 cm/s can be unambiguously extracted. This is an extremely large value, but is comparable to what has been reported in literature for unpassivated surfaces [1], [2].

All the extracted parameters of Table 5.2 (see Chapter 5) based on this experimental run is summarised in Table 6. 2, which suggests that the impact of the embedded porous silicon on the epitaxial layer effective lifetimes comes mainly in the form of increased interface recombination rather than a reduced epitaxial layer bulk quality.

Table 6. 2 Summary of extracted bulk lifetimes and effective interface recombination velocities both in areas with and without porous silicon, and with and without BSF using the sim-PL method.

	No porous silicon		Porous silicon	
	No BSF	BSF	No BSF	BSF
τ_{epi} [µs]	~80-100		~70-90	
S_{int} [cm/s]	$\sim 10^3$	$\sim 10^3$	$\sim 1.5 \times 10^5$	$\sim 10^3$

In order to verify that indeed the bulk quality of epitaxial layers grown on annealed porous silicon is comparable to that grown on pristine silicon, four consecutive runs were performed in which samples of five different epitaxial layer thicknesses (20, 25, 30, 35 and 40 µm) were made, including a 2 µm thick BSF. The measured PL intensities from these samples are plotted together in Figure 6. 10. From this, we can deduce that the run-to-run variation in the measured PL intensities is rather small, with a standard deviation of ~3-5% of the average PL intensity, for all thicknesses.

The measured PL intensities in the area without porous silicon were corrected to subtract the substrate PL contribution as described before. For run B and C, the PL intensities in the porous silicon area were also corrected because the intercept of the linear fit line had a slight positive intercept, greater than the standard deviation, indicating non-negligible substrate contribution. Since it is difficult to model the substrate contribution in this case, the correction was made by simply shifting down the data points such that the linear fit line had zero intercept. As explained before, this simplified correction could lead to a slight underestimation of the extracted bulk lifetime. For extraction of the bulk lifetime, S_{int} was assumed to $\sim 10^3$ cm/s. The extracted results from the four runs are summarised in Table 6. 3. The bulk lifetimes across the four different runs are more or less similar at ~100-125 µs and are also close to what was extracted from the first experiment (see Table 6. 2). Moreover, the bulk lifetimes of the epitaxial layers grown on top of annealed porous silicon is comparable to that grown on top of pristine silicon, ascertaining the deductions from the results of the first experiment.

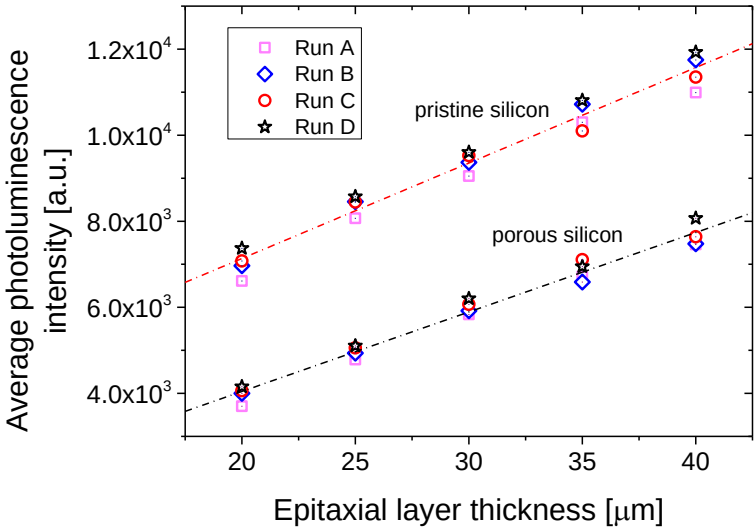

Figure 6. 10 The average PL intensities from measurements from on samples from four different runs with five different epitaxial layers thicknesses (20, 25, 30, 35 and 40 μm) both in areas with and without porous silicon. All samples have a 2 μm thick BSF shielding the interface between the epitaxial layer and the substrate. Error bars have been excluded for clarity, but are similar to the ones plotted in Figure 6. 5.

Table 6. 3 Summary of extracted bulk lifetimes both in areas with and without porous silicon, and with and without BSF using the sim-PL method.

Run	No porous silicon [μs]	Porous silicon [μs]
A	100	120
B	120	125
C	120	100
D	100	110

Next, we study epitaxial layers using μ-PCD measurements. Again, epitaxial p/p⁺ samples with thicknesses ranging from 20-50 μm in steps of 5 μm were prepared, as described in Section 6.1.1. Similar to the first experiment, two sets of samples were prepared, one with BSF and the other without. Measurements inside and outside the porous silicon area can be done on the same wafer as before.

Two typical decay transients from μ-PCD measurements on an epitaxial layer deposited on annealed porous silicon (without a protective BSF) and on pristine silicon are shown in Figure 6. 11. The plots start with a sharp increase in the voltage corresponding to photo-generation over a period of 200 ns. After the irradiation has been terminated, the excess carrier population decays and correspondingly the voltage also decays. The decay is particularly interesting because it shows two main parts: an initial slow decay and a mono-exponential tail decay. This initial decay cannot be described with a single exponential relation. Importantly, this is in stark contrast to the simulations of Walter *et al.* [3], which predicts a strong initial decay followed by a mono-exponential tail transient during

μ-PCD measurements of epitaxial p/p⁺ structures. In fact, in their measurement, they did not observe such a strong initial decay.

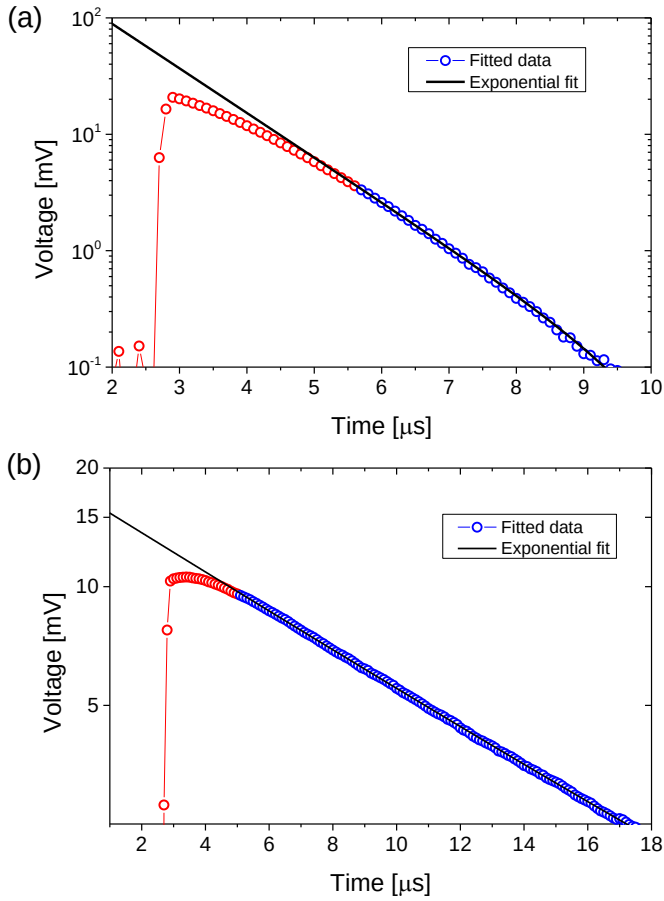

Figure 6. 11 Decay transients from μ-PCD measurements on (a) an epitaxial layer grown on embedded porous silicon layer without BSF, (b) an epitaxial layer grown on pristine p⁺ silicon. The data is blue are used for fitting an exponential function from which the effective lifetimes have been extracted to be 0.79 μs (R^2 = 0.99967) and 5.95 μs (R^2 = 0.99989) respectively.

Ogita modeled this slow initial decay in bulk wafers and attributed it to the much higher recombination at the rear surface compared to the front surface [4]. This is also the case for our epitaxial samples which usually have a higher interface recombination compared to recombination at the well-passivated front surface. To understand this, the carrier density profiles during the decay must be considered. After the illumination is turned off, two phenomena occur: (1) recombination of carriers in the bulk, at the front surface and at the interface, and (2) diffusion of carriers from the front towards the interface due to the fact that during illumination more carriers are generated closer to the front surface. Thus, in a sample with a higher interface recombination compared to front surface

recombination, there will be a stronger decrease in the carrier density after the carriers from the front surface reach the interface, resulting in a stronger decay after an initial slow decay. However, after this initial period, the carrier density profile shape does not change and the carrier density reduces uniformly everywhere. This is why the tail part of the transient can be described by a mono-exponential relation. As shown in Figure 6. 11, indeed this tail part of the decay can be fitted very well ($R^2 > 0.999$) with a mono-exponential function.

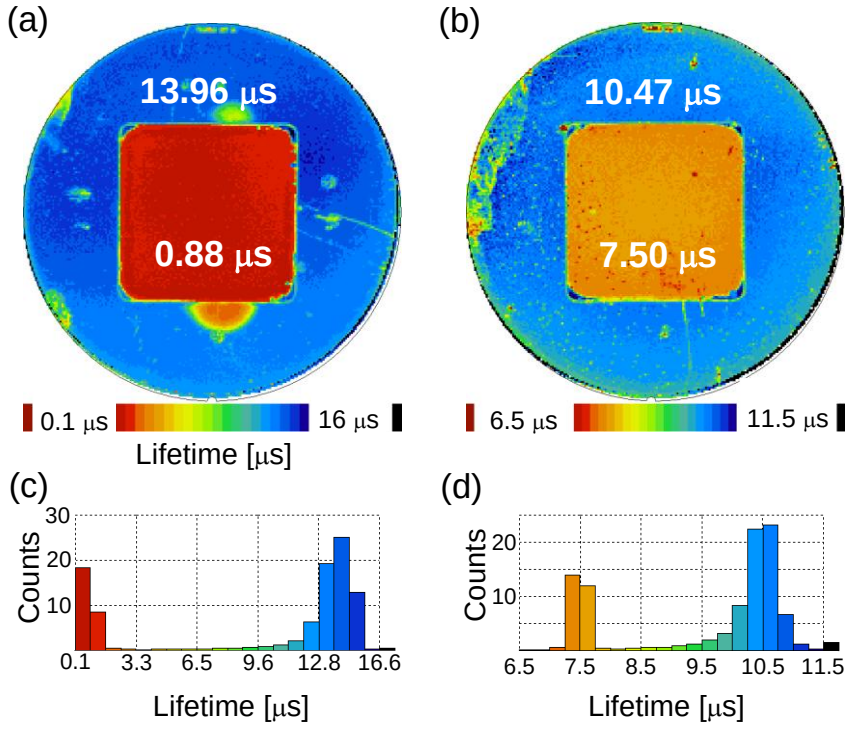

Figure 6. 12 Effective lifetime maps measured using µ-PCD for a 40 µm thick epitaxial p-type layer grown on a p^+ substrate (a) without a BSF, and (b) with a 2 µm thick BSF. (c) and (d) Histograms of the distribution of measured lifetimes corresponding to (a) and (b) respectively. In both wafers, the central area of 8.5 cm by 8.5 cm has embedded porous silicon. The values written in the maps are median effective lifetime values in the corresponding regions (inside or outside porous silicon). The raster size is 1 mm^2.

Multiple transient measurements (1024 times) on the same spot and a raster scanning of the entire wafer yields effective lifetime maps as shown in Figure 6. 12, where two samples are shown, one with BSF and the other without. The square-shaped region of ~8.5 cm by 8.5 cm in the middle of both lifetime maps with a lower effective lifetime (relative to the peripheral regions) corresponds to an epitaxial layer that is grown on embedded porous silicon, while the peripheral area is associated with an epilayer grown on pristine silicon. Thus, it is clear that the embedded porous silicon has a significant impact on the measured effective lifetime of the epitaxial layer grown on top. The forthcoming paragraphs analyse

whether this detrimental impact of the embedded porous silicon is due to a reduction in the bulk lifetime or an enhancement of the interface recombination or both.

By comparing the lifetimes in the porous silicon areas of the two epitaxial p/p^+ samples of Figure 6. 12 (one with BSF and the other without), it is clear that the embedded porous silicon results in a drastic increase in the interface recombination, which can be understood from the fact that the porous silicon voids surfaces are unpassivated and thus have a large concentration of recombination centres. The BSF, as expected, provides a potential barrier which repels minority carrier electrons in the epitaxial layer away from the recombinative porous silicon surfaces, thereby increasing the effective lifetime (~7.5 µs median value) in the sample with BSF compared to the one without it (~0.88 µs median value). This is also more clearly seen from Figure 6. 13, which shows typical line scans taken from the effective lifetime maps of Figure 6. 12. The dip in the effective lifetime in the middle is due to the embedded porous silicon. When a BSF is present, this dip is much less than the case without a BSF. A reduction in the effective lifetime in the peripheral areas when a BSF is present is also observed. This will also be briefly touched upon later.

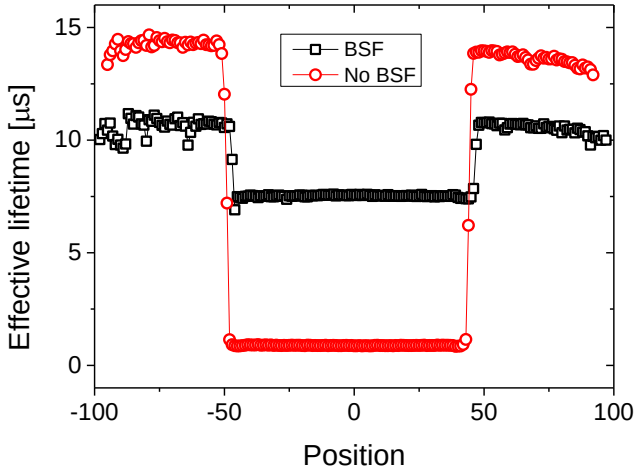

Figure 6. 13 Line scans from the effective lifetime maps of Figure 6. 12 showing the beneficial effect of porous silicon on the effective lifetime in the porous silicon area.

Effective lifetime mapping is performed on samples with different epitaxial layer thicknesses, ranging from 20-50 µm. A median is calculated based on the effective lifetime distributions from these maps, both in areas with and without porous silicon. The extracted median effective lifetimes are plotted in Figure 6. 14 as a function of epitaxial layer thickness for all four configurations. The effective lifetime increases almost linearly with the epitaxial layer thickness as can be expected from eqn. (5.15) (see Chapter 5). Expectedly, the epitaxial layers grown on pristine silicon expectedly show the highest lifetimes.

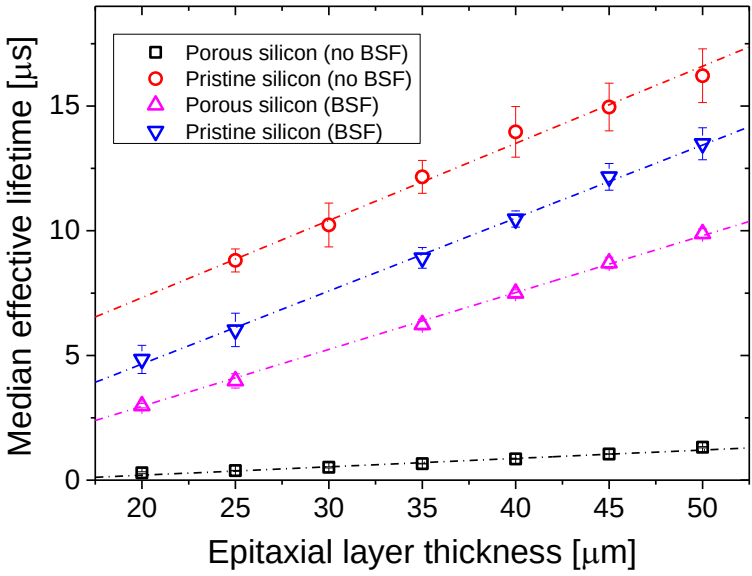

Figure 6. 14 The median effective lifetime obtained from the effective lifetime distributions in µ-PCD lifetime maps in areas with and without porous silicon are plotted for different epitaxial layer thickness for all four configurations.

A plot of the reciprocal of effective lifetime versus reciprocal epitaxial layer thickness for two of four configurations is shown in Figure 6. 15 as examples to demonstrate the extraction of S_{tot} (from the slope) and τ_{epi} (from the τ_{eff}^{-1}-axis intercept) as explained in Chapter 5, Section 5.2.2.3. Best fit lines through both sets of data show an extremely good linear fit.

The epitaxial layer grown on pristine silicon obviously has a much smaller S_{tot} of ~269 cm/s compared to the one grown on BSF-shielded porous silicon (~785 cm/s). For the case without porous silicon, for a substrate doping concentration of 10^{19} cm^{-3}, S_{BSF} can be calculated to be ~100 cm/s using eqn. (5.2) (see Figure 5.2 in Chapter 5). Assuming S_{fr} to be ~10 cm/s, $S_{defects}$ works out to be ~110 cm/s and therefore seems to be the dominant surface/interface recombination channel in the absence of BSF. For an epilayer on pristine silicon, a bulk lifetime of ~155 µs is also obtained from the intercept. This is much larger than that reported in [5]. This will be the reference to compare with for the bulk lifetime of epitaxial layers grown on annealed porous silicon, to evaluate if the bulk quality of the epilayer is adversely affected when grown on porous silicon or not. For the case of BSF-protected porous silicon, however, the high S_{tot} means that the τ_{eff}^{-1}-axis intercept is negative and it is not possible extract a bulk lifetime for this case, as also explained using Table 5.3 in Chapter 5.

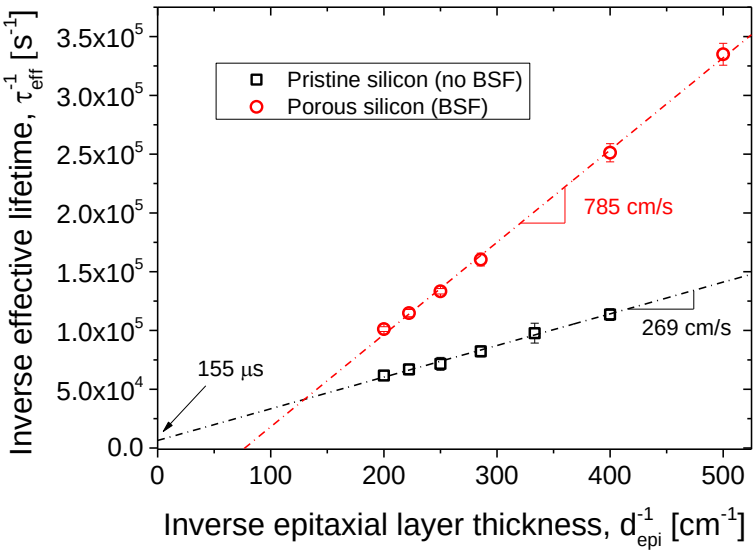

Figure 6. 15 Extraction of bulk lifetime and the sum of effective surface and effective interface recombination velocities from the τ_{eff}^{-1}-axis intercept and the slope respectively, shown for two configurations, namely, an epitaxial layer grown on pristine silicon and an epitaxial layer grown on BSF-shielded porous silicon.

Table 6. 4 Summary of extraction results of bulk lifetime and the sum of effective surface and effective interface recombination velocities from µ-PCD measurements.

	No porous silicon		Porous silicon	
	τ_{epi} [µs]	S_{tot} [cm/s]	τ_{epi} [µs]	S_{tot} [cm/s]
No BSF	155	269	negative	8940
BSF	negative	449	negative	785

These results together with similar extractions performed on the other sample sets are summarised in Table 6. 4. Unfortunately, only S_{tot} can be reliably extracted for all four configurations. It is seen that the lower effective lifetimes in epilayers grown on BSF-shielded pristine silicon is probably due to a higher S_{tot} in these samples. The reasons for this is however unclear. Finally, the S_{tot} of an unshielded p/p$^+$ interface with an embedded porous silicon is extremely high (close to 10^4 cm/s). A 2 µm thick BSF with a doping concentration of ~10^{19} cm^{-3} appears to be a very effective shield since S_{tot} is now reduced by about an order of magnitude.

As discussed in Section 5.2.3.3 in Chapter 5, while S_{tot} can be reliably extracted using µ-PCD, it is not so sensitive for extraction of τ_{epi} in epitaxial p/p$^+$ structures, particularly when the bulk lifetime is high. On the other hand, up to an S_{tot} of ~10^3 cm/s, the method of sim-PL is rather insensitive to S_{tot} but very sensitive to τ_{epi}. These differences can be traced to the fact that the former is a transient lifetime

technique while the latter is a steady-state technique with different carrier density profiles during the measurement. Since the bulk lifetime of epitaxial layers grown on porous silicon cannot be extracted using μ-PCD, the complementary method of sim-PL can be used again to extract the bulk lifetimes (see [6]) and this time, the S_{tot} values extracted from μ-PCD measurements (Table 6. 4) can be used to simulate calibration curves similar to Figure 5.6 in Chapter 5, without ambiguity. Thus, using a combination of sim-PL and μ-PCD, the bulk lifetime and effective interface recombination velocity in epitaxial p/p$^+$ structures can be well-studied.

From the results obtained thus far, firstly, it is clear that the crystal quality of the epitaxial layer grown on annealed porous silicon Bragg stack is indeed comparable to that grown on pristine silicon, since the bulk lifetimes obtained in the two areas are comparable. In some cases, the bulk lifetime in the epitaxial layer grown on top of annealed porous silicon is even higher compared to the reference. This implies that the porous silicon stack used as a Bragg reflector is indeed well-optimised for high quality epitaxial growth similar to a pristine silicon template. This is also supported by defect density measurements that were performed on defect-etched epitaxial layers, which resulted in a similar defect density in the epitaxial layers from both areas with and without porous silicon.

Secondly, occasionally, the bulk lifetime of the epitaxial layer grown on re-organised porous silicon can be higher than that grown in areas without porous silicon. This can be understood by the fact that the quality of p$^+$ substrates are not well-controlled with regards to the contamination levels. Thus, these p$^+$ substrates (despite being Cz-grown) can be relatively contaminated with transition metals because these metals are highly soluble in heavily-doped silicon. For instance, for the batch of substrates used in this experiment, typical iron and nickel concentrations obtained from glow discharge mass spectroscopy (GDMS) of the substrate material were $2.0 \times 10^{14}/\text{cm}^3$ and $2.4 \times 10^{14}/\text{cm}^3$ respectively, which is rather high for solar cells. While some metals such as copper and iron prefer to segregate to highly-doped regions, other metals such as nickel do not show such behaviour. Moreover, at high temperature the segregation coefficient is low and doping-dependent segregation only happens during cooling. Thus, it is possible that in regions without porous silicon, any transition metals that may be present could have out-diffused into the epitaxial layer, thereby lowering the epitaxial layer lifetime in comparison to the area with porous silicon.

To further assess the presence of metals in "clean" p$^+$ substrates, a secondary ion mass spectroscopy (SIMS) depth profiling analysis was also done on one of these epitaxial p/p$^+$ silicon structures used in the lifetime measurements. The result is plotted in Figure 6. 16, which shows a distinct accumulation of copper and nickel in the depth associated with porous silicon, which further supports the proposition of metal contamination in p$^+$ substrates. Therefore, the porous silicon layer effectively "cleans" up the epitaxial layer on top of it, consequently increasing the lifetime of the epitaxial layer on top. This implies that when more severely-contaminated low-cost substrates are used, the porous silicon layer is indispensable for ensuring a higher lifetime.

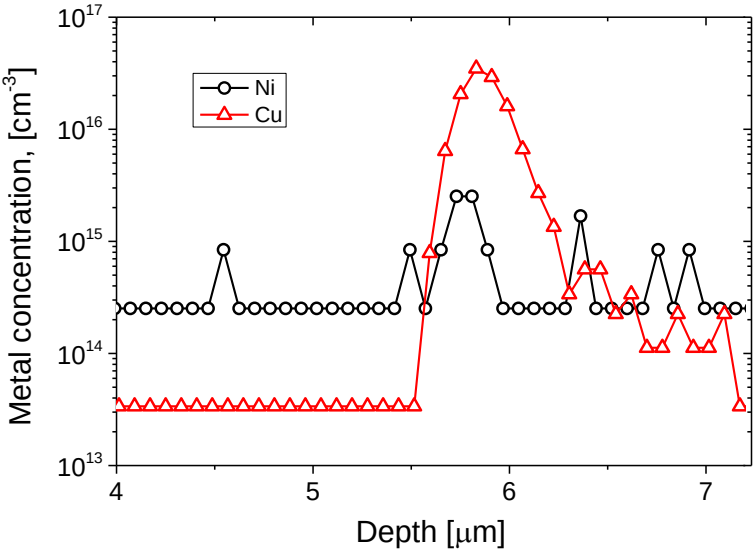

Figure 6. 16 Copper and nickel concentration in depth obtained after polishing about 22-25 μm of silicon and then performing a SIMS depth profiling.

While the porous silicon layer does not seem to have a detrimental impact on the bulk lifetime, it has a strong adverse effect on the effective interface recombination velocity. When the porous silicon interface with the epitaxial layer is not protected by a BSF, the effective interface recombination velocity is measured to in the range of 10^4-10^5 cm/s, which agrees well with that reported in literature for unpassivated surfaces [1].

Thus, a BSF is compulsory in WE-epicells to mitigate the negative effects of interface recombination on the effective lifetime. The "rough" estimation of the S_{tot} made using sim-PL shows that a 2 μm thick BSF is electronically "opaque" to minority carriers in the epitaxial layer with the S_{tot} of BSF-shielded porous silicon interface being similar to that without porous silicon. However, a more accurate analysis using μ-PCD showed that while the 2 μm thick BSF is hugely beneficial in reducing the interface recombination, the S_{tot} of BSF-shielded porous silicon interface is still 2-3 times larger than the one without embedded porous silicon.

To gain more insight into these differences theoretically, we consider again the expression for the effective surface recombination velocity of a high-low junction derived by Godlewski *et al.* i.e. eqn. (5.2). In the presence of an embedded porous silicon layer, we can consider the porous silicon layer itself as the "rear" of the p^+ region, due to the extremely high recombination expected in the unpassivated surfaces of porous silicon. We can therefore make a simplification of eqn. (5.2) assuming S_{rear} is very large and taking d_{sub} to be the distance from the low-end of the high-low junction to the embedded porous silicon, which is expressed as d_{BSF}. This yields the following expression for a high-low junction with an embedded porous silicon layer,

$$S_{BSF} = \frac{D_{sub}N_{epi}}{L_{sub}N_{sub}} \mathrm{e}^{\left(\frac{\Delta E_{G,sub}}{k_B T}\right)} \coth\frac{d_{BSF}}{L_{sub}} \quad (6.4)$$

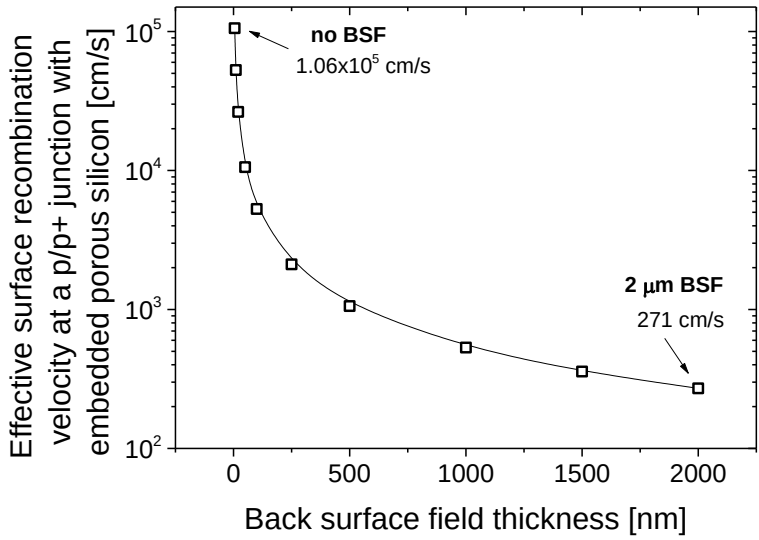

Figure 6. 17 Effective interface recombination velocity calculated according to eqn. (6.4) for different back surface field thicknesses.

The effective interface recombination velocity calculated using eqn. (6.4) for different values of d_{BSF} is plotted in Figure 6. 17. In the case of a porous silicon layer that is not shielded by a BSF, after reorganisation, there is a thin layer of p^+ silicon of about 5-10 nm thickness at the surface before epitaxial growth. Moreover, during the high temperature epitaxial growth, the dopants in this thin layer can out-diffuse into the epitaxial layer itself. Nevertheless, assuming this layer to be ~5-10 nm, then the effective interface recombination velocity obtained based on eqn. (6.4) is 5.28×10^4 – 1.06×10^5 cm/s, which is remarkably in excellent agreement with what was extracted from the experiment.

On the other hand, if the porous silicon surface is shielded by an epitaxially-grown thick BSF of 2 μm, then the effective interface recombination velocity is ~270 cm/s. We can compare this value to the one in Figure 5.2 in Chapter 5 for the substrate doping concentration of 10^{19} cm^{-3} i.e. 100 cm/s, which corresponds to the case without the embedded porous silicon. Thus, the S_{BSF} of a BSF-shielded porous silicon-epitaxial layer interface is about 2.7 times more than that without porous silicon. From Table 6. 4, we get a ratio of ~2.9 times from experiment. Again, the agreement between experiment and the analytical model is remarkable.

6.2 Lifetime measurements on detached epitaxial layers

6.2.1 Sample preparation and characterisation details

Samples for lifetime measurements were processed starting with mirror-polished, 10 cm by 10 cm square, Cz-grown, p^+ silicon wafers with a boron doping concentration of $1\text{-}2\times10^{19}$ cm^{-3}. The processing sequence until front-side passivation is similar to that for attached epitaxial layers detailed in Section 6.1.1. The main differences are the porous silicon structure and the epitaxial foil doping type. For detached epitaxial layers or foils, a porous silicon layer consisting of a low porosity template layer (LP-TL) with a porosity of ~30% on top of a high porosity detachment layer (HP-DL) with an initial porosity of ~60% is electrochemically etched on the top surface using a HF/ethanol mixture (22% HF by volume) as the electrolyte. This double layer structure is achieved by applying different current densities for the different layers: 1.4 mA/cm^2 for the LP-TL and ~73.5 mA/cm^2 for the HP-DL. The square-like etched area is approximately 8.5 cm by 8.5 cm.

The subsequent high temperature sintering at 1130 ^oC restructures the morphology of the porous silicon so that a mechanically weak detachment plane forms at the depth associated with the HP-DL, as already explained in Chapter 1. The schematic cross-section of the bi-layered (LP-TL and HP-DL) morphology of annealed porous silicon can be seen steps (1) and (2) in Figure 6. 18. A SEM image of this is also shown in Chapter 1 in Figure 1.9.

After porous silicon reorganisation, an n-type epitaxial layer with an arsenic doping concentration of 10^{16} cm^{-3} is grown in-situ, with thicknesses in the range of 30-50 µm. Only n-type detached epitaxial foils are studied in this thesis because of the expected strategic shift of the industry towards n-type solar cells. The remaining processes are illustrated schematically in sequence in Figure 6. 18. After epitaxy, the front side is passivated with a hydrogenated 10 nm thick intrinsic amorphous silicon and 20 nm thick n^+-doped amorphous silicon stack (i/n^+ a-Si:H) using plasma-enhanced chemical vapour deposition at 200 ^oC.

Out of the 8.5 cm by 8.5 cm area where porous silicon has been etched, only ~7.5 cm by 7.5 cm area is detachable (and thus usable) due to edge effects during electrochemical etching. However, for the lifetime measurements, only an area of ~6.3 cm by 6.3 cm is used. This area is defined by laser ablation of silicon from the top surface through the entire epitaxial layer until the LP-TL is reached. This step is not shown in Figure 6. 18. At this stage, the epitaxial foil is still attached to the parent substrate, albeit weakly, by the remaining LP-TL and the interconnections/pillars in the HP-DL.

Once the foil area has been defined, a 6 cm by 6 cm area of silicone with a thickness of ~120 µm is stencil-printed on a cleaned piece of glass. The silicone used is a 2-component adhesive ("PV6100 Cell encapsulant", provided by Dow Corning). Note that the area of silicone is slightly smaller than the area of the epitaxial foil defined by laser grooving. After 15 min of curing in vacuum at 100 ^oC,

the glass is then bonded to an epitaxial foil that is still attached to the substrate with silicone as the glue (step (4) in Figure 6. 18). Subsequently, the silicone is further cured for 1-2 hours in vacuum at 200 ^{o}C and then cooled gradually to room temperature. Subsequently, ultrasonication for a few minutes in a water bath at room temperature is done to detach the epitaxial foil from the parent substrate (step (3) in Figure 6. 18).

As outlined in Table 5.1 in Chapter 5, the presence of silicone presents a challenge for the next two processing steps: the removal of residual porous silicon and the passivation of the rear-surface. The residual porous silicon belonging to the annealed LP-TL must be removed using a silicon etchant that does not react strongly with the silicone. Moreover, silicone should not be directly exposed to the plasma during amorphous silicon deposition, because it will lead to very poor surface passivation [7]–[9].

In order to minimise the problems associated with silicone, a shielded configuration (i.e. the area of the epitaxial foil is greater than the area of the printed silicone) is used. However, in this configuration, silicon flaps (i.e. the overhanging regions of the epitaxial foil that is not supported by the silicone) that exist all around the edges of the foil are fragile and can easily break during wet processing and drying. Moreover, cracks can form and propagate into the foil. These can lead to exposed areas of silicone, which must be dealt with before further processing.

Therefore, besides using a shielded configuration, a dielectric is also frequently used to cover the exposed silicone areas during the processing of the epitaxial foils for lifetime measurements (step (4) in Figure 6. 18). This dielectric mask is a stack of silicon dioxide of ~165 nm and silicon nitride of ~75 nm deposited by PECVD at 225 ^{o}C using a shadow mask (a piece of glass) to cover areas which will be eventually passivated with amorphous silicon. In this way, any silicone that is exposed inadvertently is shielded during further processing and thus does not affect the quality of the passivation.

Tetramethyl ammonium hydroxide (TMAH) diluted in water to a concentration of ~5% by volume was found to be suitable for removing the residual porous silicon. The etching is done at ~70-85 ^{o}C, resulting in etch rates for porous silicon of ~400-500 nm/min. Vigorous bubbling is observed during porous silicon etching, and the effervescence diminishes suddenly once the bulk silicon of the epitaxial foil is reached. An over-etch of 1 min is used to produce a shiny, smooth surface for better passivation (step (5) in Figure 6. 18). It should be noted that TMAH does react with silicone but much less aggressively than other mixtures such as the commonly-used CP8 mixture (nitric acid: hydrofluoric acid: acetic acid = 8:1:1). In addition, in the shielded configuration, the reaction of TMAH with silicone is minimised by geometry. After TMAH etching, the sample undergoes a very short HF dip of 2-3 seconds.

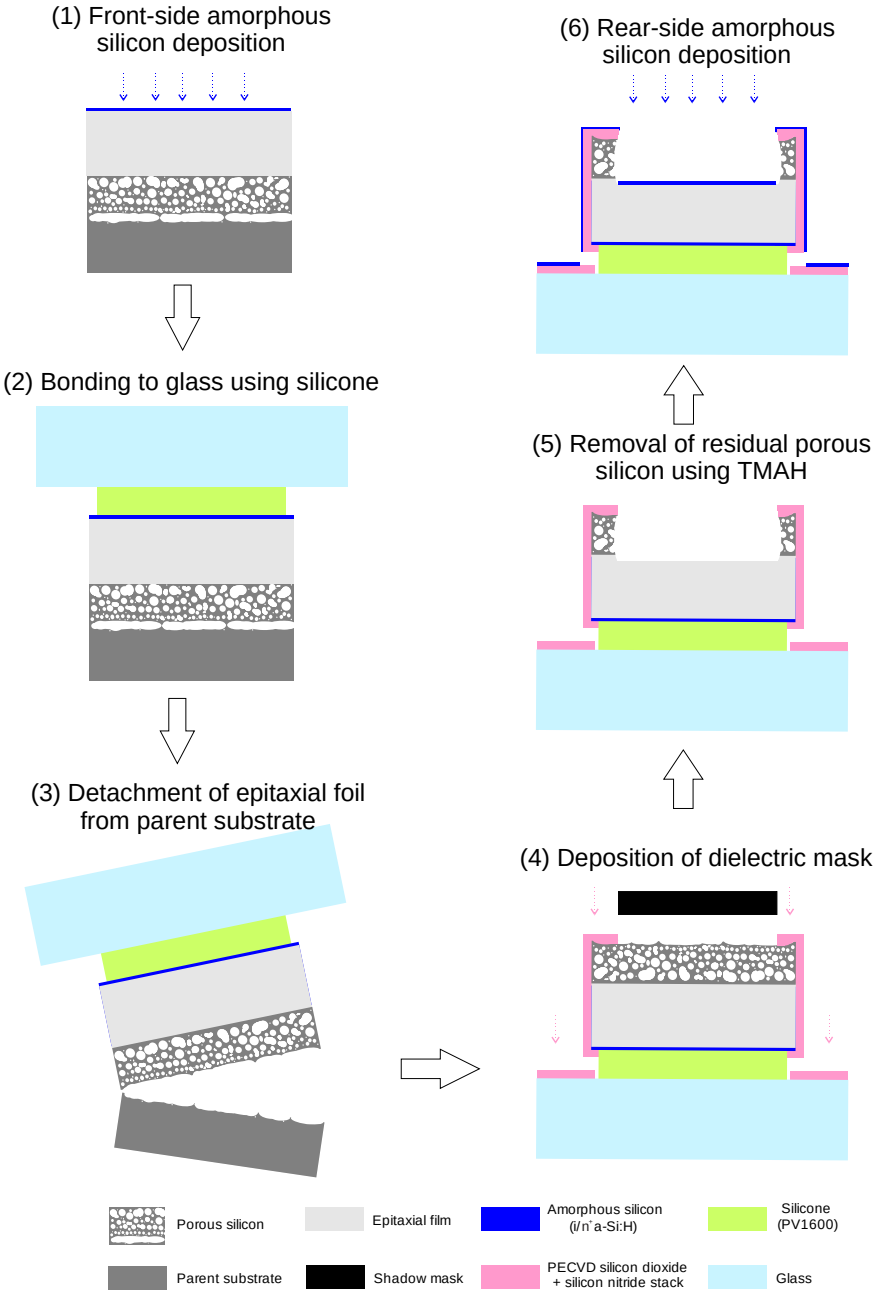

Figure 6. 18 Schematic diagrams depicting the process sequences used in the preparation of glass-bonded epitaxial foils for lifetime measurements. A dielectric mask is used to cover areas of exposed silicone. The diagrams are not drawn to scale and relative sizes of the epitaxial foil and porous silicon are exaggerated for clarity.

Finally, the rear surface of the epitaxial foil is passivated with the same i/n⁺ a-Si:H stack used for front-side passivation. Minority carrier lifetime measurements are then performed on these passivated samples using the commercially available PL imaging tool (LIS-R1) from BT Imaging in which both quasi-steady state photoconductance measurements (QSSPC) as well as photoluminescence (PL) measurements can be performed. This set-up is schematically shown in Figure 6. 19. The samples were illuminated from the side of the glass. The optical absorption losses in the glass, glue and amorphous silicon stack are negligible [10] and hence neglected in the analysis. A photograph of a passivated, glass-bonded epitaxial foil is shown in Figure 6. 20.

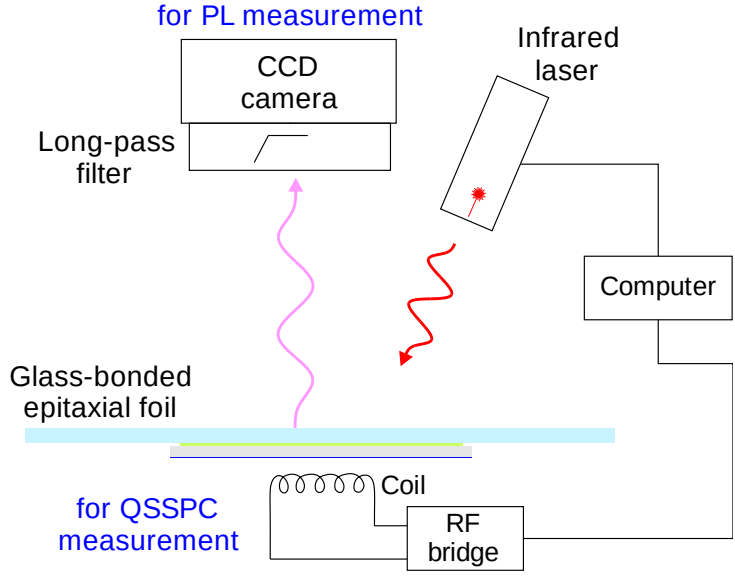

Figure 6. 19 A schematic diagram of the measurement set-up used for characterising the minority carrier lifetime of epitaxial foils. Both photoluminescence (PL) measurements and quasi-steady state photoconductance (QSSPC) measurements can be done with this set-up. The PL set-up is similar to that explained in Figure 6. 2. The PL image can be calibrated using the QSSPC measurement to obtain calibrated PL images. The sample is illuminated through glass.

For lifetime measurements on attached epitaxial layers, the epitaxial layers grown on pristine silicon acted as appropriate reference. For the detached epitaxial foils, lithography-based epitaxial foils were used as reference. For these reference foils, the electrochemical etching of mesoporous porous silicon is replaced by dry etching of macro-pores patterned by deep-ultraviolet (DUV) lithography. This is based on the empty-space-in-silicon technique introduced by Mizushima, Sato *et al.* [11] and extended for solar cell applications by Depauw et al. [12]. An array of ~500 nm wide holes with a half-pitch length of ~400 nm are patterned by DUV lithography. These holes were then dry-etched to a depth of ~3.2 µm, resulting in large macro-pores as shown in Figure 6. 21 (a). A subsequent anneal at 1130 °C for ~5-10 min results in coalescence of all the pores into one long empty space in silicon as shown in Figure 6. 21 (b). Remarkably, the 1 µm

thick layer of silicon sealing this long cavity is crystalline and completely free of voids, presenting an ideal surface for epitaxial growth and effortless detachment. Epitaxial foils grown on lithography-based templates will therefore stand as references for the epitaxial foils grown on porous silicon-based templates.

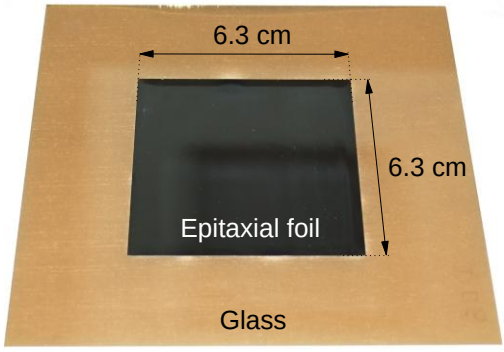

Figure 6. 20 Photograph of a glass-bonded epitaxial foil. The brownish tinge around the epitaxial foil is due to the amorphous silicon deposited on glass.

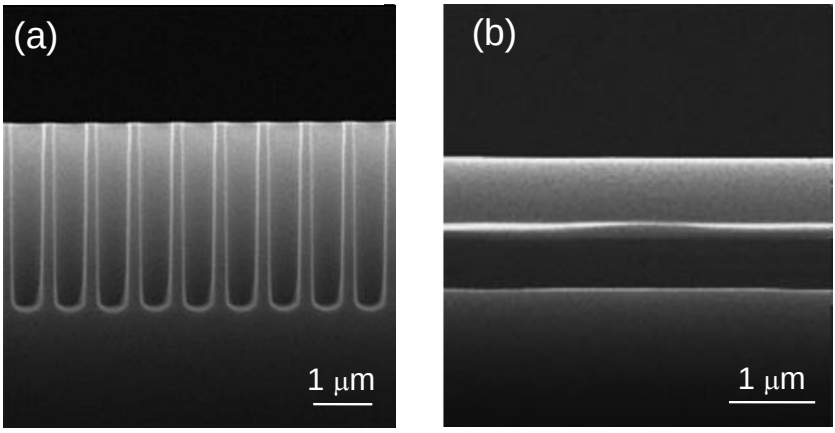

Figure 6. 21 Cross-sectional SEM images of (a) regularly macro-pores formed by dry etching after DUV lithographic patterning of an array of ~500 nm diameter holes with a half pitch length of ~800 nm, and (b) the same sample after annealing at 1130 °C resulting in the coalescence of the macro-pores and formation of a long empty space sealed by a dense void-free silicon layer of ~1 μm [12].

6.2.2 Experimental results and discussion

To start with, the complications of processing epitaxial foils into reliably-passivated samples for lifetime measurements are illustrated. Starting with large batches of samples, due to yield loss issues at various process steps, only few epitaxial foils survive at the end of the process sequence. Two n-type, 40 μm thick, epitaxial foils that were successfully detached from their parent substrates were processed according to the sequence shown in Figure 6. 18, with the exception of

the dielectric mask. Both samples had macroscopic cracks propagating into the epitaxial foil, starting from defects on the overhanging flaps on the edges. In some cases, parts of the overhanging flaps which shield the silicone were broken, resulting in areas or edges with exposed silicone which are prone to attack by TMAH during porous silicon removal or by the plasma during a-Si deposition.

The resulting lifetime images of these samples are shown in Figure 6. 22. Firstly, the effective lifetime values in both samples are generally very low (<20 µs). The lifetime images show quite some inhomogeneities with particularly low lifetimes in and around the edges, cracks and areas of exposed silicone. Very low lifetimes are measured even a few centimetres away from the cracks and edges. Thus, it is clear that exposed silicone has a strong detrimental impact on the measured effective lifetime of epitaxial foils.

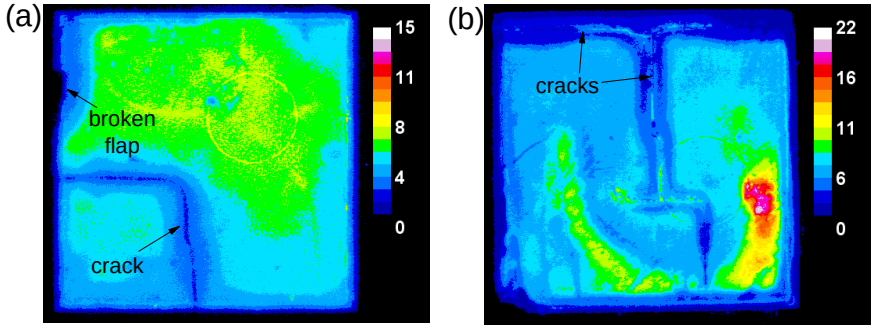

Figure 6. 22 Lifetime maps of two 40 µm thick n-type epitaxial foils, passivated with i/n⁺ a-Si:H. These maps based on photoluminescence (PL) images calibrated by quasi-steady state photoconductance, with the calibration point for (a) taken at an injection level of 4.4×10^{14} *cm⁻³ and for (b) taken at* 6×10^{14} *cm⁻³. Cracks going through the epitaxial foils are clearly visible.*

These examples highlight two important problems which are very typical with regards to processing epitaxial foils. Firstly, the yield and reliability of the detachment process is crucial for the high-volume production of high quality epitaxial foils with high quality passivation. Secondly, the detrimental effects of silicone in terms of surface passivation must be taken care of so that surface recombination can be minimised and the bulk quality of the epitaxial foils can be studied.

The first problem is treated in Chapter 7, where a method is proposed to enable reliable detachment. The latter problem is solved in two ways: (1) the use of a dielectric mask as depicted in Figure 6. 18, and (2) locally modifying the silicone in exposed areas such that it becomes inert during porous silicon removal and a-Si deposition. This has been achieved by exposing the sample to oxygen plasma which modifies the chemical structure of exposed silicone, rendering it harmless for the next process steps [8]. Both methods are very effective and only the first technique of dielectric masking is used in this thesis.

In another experimental run, two porous silicon-based epitaxial foils and one lithography-based epitaxial foil were processed without any cracks and with

dielectric masking of the edges. The resulting lifetime maps for the two porous silicon-based epitaxial foils are shown in Figure 6. 23. The measured effective lifetimes are much higher than those in Figure 6. 22, demonstrating that the surface recombination velocity can be suppressed if exposed silicone areas are shielded during processing. This allows the study of the bulk quality of epitaxial foils. The lifetime values in Figure 6. 23 (b) are higher than those in Figure 6. 23 (a) because the latter is a thinner epitaxial foil.

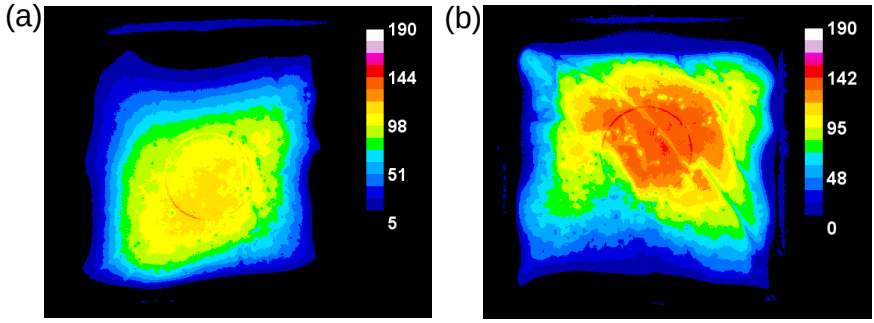

Figure 6. 23 Lifetime maps of (a) 40 µm thick, and (b) 50 µm thick n-type epitaxial foils, passivated with i/n⁺ a-Si:H. These maps based on photoluminescence (PL) images calibrated by quasi-steady state photoconductance, with the calibration point taken at an injection level of 6×10^{15} *cm⁻³. Dielectric masking has been used for the edges.*

It can also be observed that the edges are not well-defined, compared to those in Figure 6. 22 because the shadow mask used in step (4) of Figure 6. 18 allows some deposition of the dielectric under the mask. The extent and thickness of this under-deposition depends on the waviness of the epitaxial foil surface. Even a very thin layer of dielectric retards or completely masks the removal of porous silicon underneath during TMAH etching. Therefore, the central areas of the foils are best for comparison.

Injection level-dependent lifetime curves from QSSPC measurement in the middle of the three epitaxial foils (two porous silicon-based foils and one lithography-based foil) are shown in Figure 6. 24. The lifetime of the lithography-based epitaxial foil is considerably higher than the porous silicon-based epitaxial foils. Since the passivation scheme and processing steps are the same for both types of epitaxial foils, it can be deduced that this difference in effective lifetime is largely due to a difference in the bulk quality of the epitaxial foils. This can be traced to the quality of the starting template on which epitaxy is performed. In the case of porous silicon-based epitaxial foils, the growth template is the surface of the reorganised LP-TL, which has several enclosed voids of various dimensions throughout the layer. On the other hand, for the lithography-based epitaxial foils, the growth template is a void-free layer of dense crystalline silicon. In Chapter 7, this is further analysed and methods to improve the quality of porous silicon-based epitaxial foils are proposed.

Next, in order to evaluate the bulk lifetime of the epitaxial foils, the typical surface recombination velocity of glass-bonded epitaxial foils must be evaluated

first. For this, several n-type FZ wafers with a thickness of ~280 μm were used. Firstly, these wafers were down-sized by laser ablation into samples with an area of 6.3 cm by 6.3 cm. These samples then went through the same processing steps that a typical epitaxial foils goes through, namely, front-side a-Si deposition, bonding, curing, TMAH etching, cleaning and rear-side a-Si deposition. Since the bulk lifetime of FZ wafers exceed 1 ms, the effective lifetime measured on these samples was equated to the surface lifetime. The calculated S_{tot} is very low (<10 cm/s), indicating that high quality passivation is possible on glass-bonded silicon wafers.

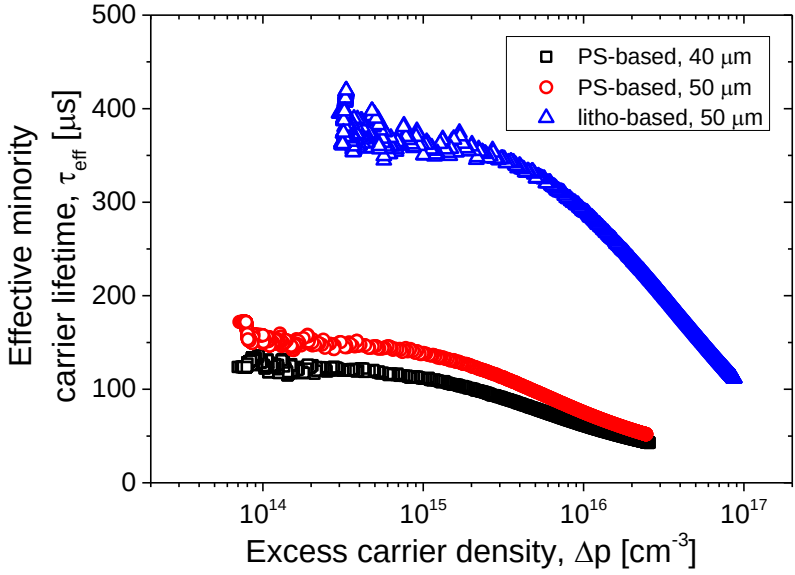

Figure 6. 24 Injection level-dependent effective lifetimes of two porous silicon-based epitaxial foils (40 and 50 μm) and a lithography-based epitaxial foil (50 μm), showing considerable difference in epitaxial quality between the two types. "PS" refers to "porous silicon" and "litho" refers to "lithography".

From the calculated S_{tot}, the bulk lifetime of the n-type epitaxial foils of Figure 6. 24 can be evaluated using eqn. (5.47) (see Chapter 5). Taking the effective lifetime at the injection level of 10^{15} cm^{-3}, the bulk lifetime has been calculated for three different S_{tot} values and tabulated in Table 6. 5. If S_{tot} is similar to that obtained with the reference FZ wafers, then the bulk lifetimes for the porous silicon-based epitaxial foils would be ~120-150 μs, while that of the lithography-based epitaxial foil would be ~440 μs. This would constitute the lower limit for the bulk lifetimes. This is because the S_{tot} values for the actual epitaxial foils would be expected to be higher than those obtained from the FZ reference samples, owing to the fact that the rear surface of the epitaxial foil is bound to be rougher despite a 1 minute over-etch compared to that of the FZ wafer, because in the case of the epitaxial foil, it is porous silicon that is etched and not a mirror-polished surface. Moreover, the doping concentration of the FZ wafers are lower than that of the

epitaxial foils. For these reasons, one may expect a higher S_{tot} value for epitaxial foils.

Table 6. 5 Summary of the bulk lifetimes calculated based on eqn. (5.47) for two porous silicon-based epitaxial foils (40 and 50 μm) and a lithography-based epitaxial foil for three different values of S_{tot}. The effective lifetime was taken at an injection level of 10^{15} cm^{-3}.

	Effective lifetime at $\Delta p=10^{15}$ cm^{-3}	Bulk lifetime [μs]		
		$S_{tot} = 3$ cm/s	$S_{tot} = 6$ cm/s	$S_{tot} = 10$ cm/s
PS-based epifoil (40 μm)	~111	~120	~130	~150
PS-based epifoil (50 μm)	~139	~150	~170	~190
Litho-based epifoil (50 μm)	~350	~440	~600	~1170

Regardless of the actual value of S_{tot}, several important deductions can be made. Firstly, the porous silicon-based epitaxial foils have much lower minority carrier lifetimes compared to lithography-based epitaxial foils which act as reference layers. In comparison, the attached epitaxial layers grown porous silicon Bragg reflectors have lifetimes comparable to that of the reference epitaxial layers grown on pristine silicon.

Based on Coletti's work, a minority carrier diffusion length that is 15-20 times the silicon thickness would be needed to attain close to the maximum possible efficiency [13]. Bulk lifetimes of ~100-120 μs in p-type attached epitaxial layers translate to ~535-600 μm minority carrier diffusion lengths, which are indeed 10-15 times the thickness of the epitaxial layer. However, the bulk lifetimes in excess of 320 μs are needed in n-type epitaxial foils to attain diffusion lengths in excess of 600 μm, which is clearly not the case for porous silicon-based epitaxial foils, as shown in Table 6.5.

From this, we can conclude that the porous silicon Bragg reflector stack is not only optimised for its reflection properties but also for epitaxial growth. On the other hand, the porous silicon stack used for layer transfer is not optimal for epitaxial growth. This clearly indicates that there is a large scope for improvement of the bulk quality of detached epitaxial foils, which serves as the motivation for Chapter 7.

6.3 Chapter summary

- Minority carrier lifetime measurements on epitaxial layers attached to a p^+ silicon substrate were carried out using the two methods which were theoretically described in Chapter 5, namely, simulation-assisted photoluminescence (sim-PL) and microwave-detected photoconductance decay (μ-PCD).
- Simulation-assisted photoluminescence (sim-PL) on p-type attached epitaxial layers:

- PL intensity increased with increasing epitaxial layer thickness, which implies that epitaxial layer lifetimes were in the regime where sim-PL would work.
- As predicted by modeling, it was shown that for epitaxial layers without an embedded porous silicon layer, there was significant PL signal from the substrate which needed to be corrected. However, for the case of epitaxial layers with an embedded porous silicon layer, the substrate PL was suppressed.
- Different sets of solutions of (τ_{epi}, S_{int}) were obtained depending on the assumption made about S_{int}.
- Two different methods were presented to discriminate the correct solution set (τ_{epi}, S_{int}).
- In the first method, a μ-PCD measurement was made to measure the ballpark number for the effective lifetime, from which the correction solution set can be derived.
- In the second method, the ratio of PL intensities on areas with and without porous silicon on the same wafer was considered and approximated to be equal to the ratio of interface recombination velocities (eqn. (6.3)), under certain assumptions. This, together with modeling, was used to arrive at the correction solution set.
- Bulk lifetimes extracted in this way in epitaxial layers grown on annealed porous silicon as well as pristine silicon were comparable at ~100-125 μs i.e. 535-500 μm diffusion length. This shows that the annealed porous silicon Bragg stack does not affect the epitaxial layer quality detrimentally and is an excellent template for epitaxial growth.
- However, the effective interface recombination velocity of an unshielded p/p^+ interface with an embedded porous silicon was estimated to $\sim 1.5\times10^5$ cm/s, which is extremely high, similar to that of an unpassivated surface.
- When the interface is shielded by a 2 μm-thick back surface field (doping concentration of 10^{19} cm^{-3}), S_{int} improves to $\sim 10^3$ cm/s, comparable to an interface without an embedded porous silicon layer.

- Microwave-detected photoconductance decay (μ-PCD) on p-type attached epitaxial layers:
  - With this technique, due to the very high S_{tot} in structures with porous silicon and the comparatively high epitaxial layer bulk lifetimes, bulk lifetimes could not extracted reliably. However, accurate values for S_{tot} could be obtained.
  - A bulk lifetime of ~155 μs was obtained for a reference epitaxial layer grown on pristine p^+ silicon. Bulk lifetimes for other cases could not be extracted.

  - The S_{tot} of an of an unshielded p/p$^+$ interface with an embedded porous silicon was extracted to be ~10^4 cm/s, which is again similar to values reported for unpassivated surfaces in literature.
  - When a 2 µm-thick back surface field (doping concentration of 10^{19} cm^{-3}) shields the interface, an S_{tot} of ~800 cm/s is obtained, agreeing well with results from sim-PL.
- An analytical model to describe a p/p$^+$ junction with an embedded porous silicon was derived (eqn. (6.4)) which is well-fitted by the experimental results of S_{int}.
- Quasi-steady state photoconductance on detached n-type epitaxial foils:
  - Epitaxial foils were measured in a glass-bonded configuration.
  - It is shown that exposure of silicone during post-bonding processing steps leads to poor passivation. This would make effective lifetime an unreliable figure of merit.
  - Thus, a process sequence is described in which the silicone is shielded by a dielectric stack such that high quality passivation is possible.
  - Effective lifetime measurements on epitaxial foils resulted in much lower values for porous silicon-based epitaxial foils in comparison to lithography-based epitaxial foils (Table 6.5). In addition, a bulk lifetime in excess of ~320 µs is needed in order to attain high efficiencies based on n-type epitaxial foils, which is clearly not the case for standard porous silicon-based epitaxial foils.
  - This shows that the porous silicon stack used for layer transfer is not optimised for high quality epitaxial growth.

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Chapter 7
Enhancement of the quality of epitaxial foils

From Chapter 6, there are clear indications that for the particular case of epitaxial foils, the porous silicon properties have a strong influence on the quality of the epitaxial foil. Thus, this chapter is focused only on epitaxial foils and how the properties of porous silicon can be tuned to produce a better template for epitaxial growth and thus a higher quality epitaxial foil.

7.1 Tuning porous silicon properties towards higher lifetime epitaxial foils

As explained in Chapter 5, Section 5.1.1, there are several ways in which porous silicon can affect the quality of the epitaxial layer grown on top of it. In summary, the surface topography, intrinsic stress distribution and detachability of porous silicon would have an influence in the quality of the epitaxial foil. Since it is the surface of the low porosity template layer (LP-TL) that acts as the seed for epitaxy, particular focus is placed on tuning the properties of the LP-TL, to understand how a better porous silicon template can be created.

In Chapter 5, it was also seen that the bulk lifetimes of attached epitaxial layers were close to that of the reference layers grown on pristine p^+ silicon. The reason for this is that the porous silicon in WE-epicells are tuned for optics, while that used for layer transfer in LT-epicells is tuned for reliable detachment. As a result, void sizes in the LP-TL are much larger than those in the embedded porous silicon layer of WE-epicells. This provides the clue for the improvement of the epitaxial growth template for epitaxial foils. The effect of varying the LPL thickness and porosity on the morphology and microstructure of the porous silicon, the stress distribution inside the porous silicon, the crystal defect density of the epilayer and the lifetime of the epifoils is analysed and explained in the coming sections.

7.1.1 Sample preparation and experimental method[1]

All epitaxial foils were prepared in a similar manner to that described in Chapter 6, Section 6.2.1. Some differences and additional details are mentioned here.

Firstly, during porous silicon formation, the thickness of the etched porous silicon is modified to control the void size and void alignment in the LP-TL after reorganisation. The thickness of the LP-TL was varied by varying the etching time between 40s and 13 min, resulting in LP-TLs of thicknesses between 160 nm and 2100 nm. In two of the samples, a third layer of porous silicon of a slightly different porosity was added on top of a typical double layer structure.

Following this, the samples were thermally treated at 1130 ^{o}C in hydrogen ambient at atmospheric pressure for 10 min. In one set of samples, no epitaxial layers were grown. In the other set, 40 or 50 µm-thick, n-type silicon epitaxial layers with an arsenic doping concentration of 10^{16} cm^{-3} were grown using atmospheric pressure chemical vapour deposition (APCVD) with trichlorosilane as the precursor.

Both types of samples were inspected using the Nova™ NanoSEM scanning electron microscope (SEM) to image the morphology of the different annealed porous silicon layers. From this, the median void size at the LP-TL surface is evaluated.

On the samples without an epitaxial layer, stylus-based high-resolution profilometry measurements were performed on the LP-TL surface using HRP-200 (distributed by KLA Tencor), in order to analyze the local surface roughness of the growth surface after sintering. A typical scan length of ~20 µm was used and more than 20 profiles were measured in each sample. On two of these samples, high resolution X-ray diffraction (HR-XRD) measurements were performed using Metrix-L (distributed by Bede Scientific) by irradiating the (100) plane of the wafer surface with the Cu K-alpha1 emission line with a wavelength of 1.54056Å, and measuring the (004) Bragg reflection.

Some of the samples with an epilayer were defect-etched using the Wright etch solution [1] in order to calculate the crystal defect densities of the epitaxial layers grown on different porous silicon templates. The defect-etched samples were inspected using an optical microscope with a differential interference contrast (DIC) setup in order to visualise and count the defects.

Two of the epilayer samples were also analyzed in cross-section using a LabRam micro-Raman spectrometer with a laser of 514.5 nm wavelength to measure the stress distribution in the two porous silicon layers in cross-section.

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[1] Throughout this work, the processing procedure was continually optimised and tuned to improve the surface passivation (for e.g. improved cleaning procedure, dielectric masking of exposed silicone and improved a-Si recipe). In addition, the epitaxial deposition conditions (e.g. chamber etches and extended high temperature anneals between wafers) were also improved to grow higher quality epitaxial layers. These have resulted in continuous improvements in the effective lifetime measured over the course of the different experiments in this thesis. This background work will not discussed in this thesis. However, it is important to mention this because, in principle, it is not accurate to compare lifetime measurements across different runs. Thus, reference samples are always included for appropriate comparison. Within each graph, the data are comparable.

The remaining epitaxial layer samples were passivated as described in Figure 6.18 in Chapter 6 for minority carrier lifetime measurements.

7.1.2 Control of porous silicon morphology, topography and stress

7.1.2.1 Sintering and reorganisation of porous silicon during high temperature treatment

Various theories exist to explain the restructuring of porous silicon upon heat treatment. A commonly-used theory is the classical sintering theory, which explains the reorganisation of porous silicon by means of vacancy diffusion processes driven by a vacancy concentration gradient between the pore (or void) and its surrounding lattice. Voids grow or shrink in size depending of the direction of this vacancy gradient. The direction of the vacancy gradient depends on the vacancy concentration at the rim of the pore or void, $C_{v,void}$, relative to the lattice vacancy concentration, $C_{v,L}$. The vacancy concentration at the rim of a void of radius, r, is given by [2]

$$C_{v,void} = C_{v,0}\left(\frac{2\gamma}{r}\frac{V_0}{k_B T} + 1\right) \tag{7.1}$$

where $C_{v,0}$ is the equilibrium lattice vacancy concentration in silicon at temperature T (in Kelvins), γ is the surface tension coefficient, V_0 is the intrinsic vacancy volume in silicon and k_B is the Boltzmann constant. From this relation, it is clear that the vacancy concentration surrounding a larger void is smaller. Due to this, there exists a critical void radius, r_c, beyond which voids grow in size and below which voids shrink and disappear depending on the direction of the vacancy gradient i.e. the vacancy gradient changes sign at r_c. From a thermodynamics point of view, this is equivalent to the Ostwald ripening [3]–[5] phenomenon in solid solutions, which describes the dissolution of material from smaller particles and the accompanying redeposition onto larger particles. In the case of porous silicon, these "particles" are voids or pores and the material is vacancies.

According to Ott *et al.*, this critical radius is inversely proportional to the lattice vacancy supersaturation, $\Delta C_{v,L}$, which is defined as the excess lattice vacancy concentration above the equilibrium value at temperature T [6] i.e.

$$r_c \propto \frac{1}{\Delta C_{v,L}} = \frac{1}{C_{v,L} - C_{v,0}} \tag{7.2}$$

where $C_{v,L}$ is the lattice vacancy concentration. The lower the supersaturation, the higher the critical radius. As a result, as thermal reorganisation proceeds and the overall vacancy supersaturation in the porous silicon reduces, the average void size increases throughout the porous silicon stack. From a thermodynamics point of view, the driving force is the minimisation of free energy, which results in the minimisation of the total internal surface area of porous silicon and hence the total surface energy.

Ghannam *et al.* have argued that the minimisation of free energy should include not only the surface energy term but also strain energy associated with stress present in porous silicon. To account for this, they proposed a stress induced diffusion model which explicitly accounts for any stress that may be present in

porous silicon, such as the intrinsic stress in as-etched porous silicon, the thermal stress due to mismatch in the thermal expansion coefficients between crystalline silicon and porous silicon as well as external pressure [7], [8]. Ott *et al.* indirectly accounted for this by introducing an additional vacancy concentration term which depends on external pressure [6].

The residual stress, σ_0, in as-etched porous silicon, with cylindrical pores of radius, r, is given by [9]

$$\sigma_0(x) = \frac{r^2}{x^2}\Delta P \tag{7.3}$$

where x is the distance from the centre of the pore and ΔP is the Laplace pressure which is defined as the difference between the inner and outer pressure exerted on the surface of a pore. Such a pressure exists due to the presence of silicon hydrides on the surface of porous silicon [9], [10]. Thus, pores of larger radius (for example in the HP-DL) would have larger residual stress compared to the thinner pores. Moreover, the stress reduces with increasing distance from a pore centre.

Based on this stress-induced vacancy diffusion model, the critical radius is given by

$$r_c = \frac{2\gamma}{\sigma} \tag{7.4}$$

where γ is the surface energy density and σ is the stress in the surrounding lattice (which includes the residual stress σ_0 and other external stresses). In agreement with eqn. (7.2), this equation also predicts an overall increase in the void size as the strain in the porous silicon is relieved as reorganisation proceeds.

Finally, Ghannam *et al.* also asserted that accounting for the stress is crucial in explaining the formation of the elongated space in the HP-DL, since vacancy diffusion models can only predict the speroidisation of cylindrical as-etched pores into approximately spherical voids [7]. Stress in porous silicon is associated with a dimensionless number, Λ, which is defined as follows

$$\Lambda = \frac{\sigma^2 r}{\gamma E} \tag{7.5}$$

When $\Lambda \geq 1.39$, the critical stress is exceeded. Under such conditions, spheroidal voids would be unstable and become oblate, resulting in the rapid coalescence of the voids of the HP-DL into a long extended slit of empty space. Here E is the Young's modulus.

In short, several theories show that voids tend to get bigger under temperature treatment. This is used in the following section to understand porous silicon reorganisation.

7.1.2.2 Annealed porous silicon microstructure and topography

The cross-sectional scanning electron microscope (SEM) images of three epitaxial foil samples fabricated as explained above with three different LP-TL thicknesses (160, 290 and 720 nm) are shown in Figure 7. 1 (a)-(c).

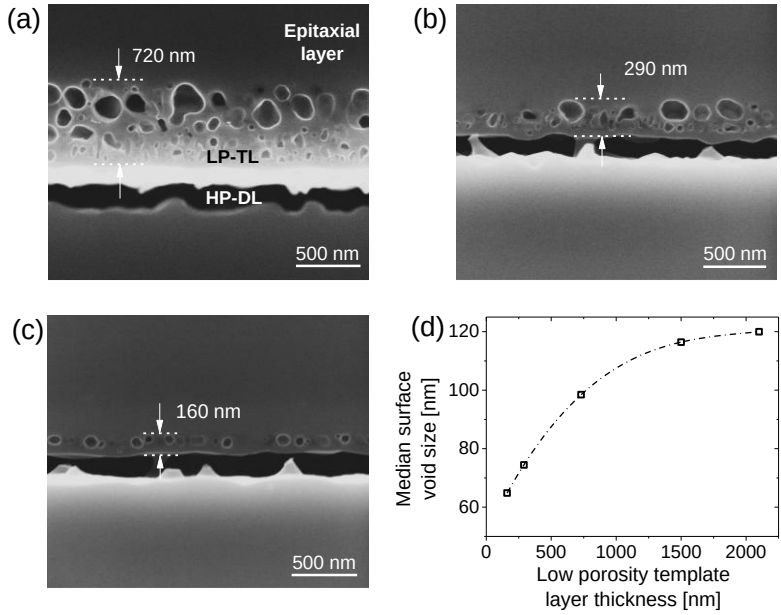

Figure 7. 1 Cross-sectional SEM images showing an epitaxial layer grown on top of a stack of porous silicon of two different porosities with (a) having a 730 nm, (b) 290 nm, and (c) 160 nm thick LP-TL. (d) A plot depicting the correlation between the LP-TL thickness and the median surface void size.

Firstly, we can notice that the two samples with thicker LP-TLs show a distribution of decreasing void sizes in depth, with the voids closer to the HP-DL being much smaller than those close to the epitaxial layer. This can be explained based on the understanding from the previous section. For the work of this chapter, the simple vacancy diffusion model appears to be adequate to explain most of the observations about the microstructure of the annealed porous silicon samples. The top surface of the porous silicon layer is a vacancy sink with the vacancy concentration close to the thermodynamic equilibrium (C_0). This results in a steep vacancy gradient that sharply reduces the vacancy supersaturation in the porous silicon close to the top surface. This in turn increases the critical void radius (see eqn. (7.2)) near the porous silicon surface, resulting in an overall increase in the sizes of the voids there. As the near-surface vacancy supersaturation reduces further, a vacancy gradient develops from deeper in the porous silicon towards the surface, resulting in a continued growth of voids near the surface, and then subsequently deeper and deeper in the porous silicon. This eventually results in a distribution of smaller and smaller void sizes deeper into the porous silicon layer. A similar vacancy gradient also exists between the LP-TL and the HP-DL which drains vacancies from the LP-TL at the interface region, resulting in the further accentuation of this void size distribution in depth. The higher starting residual stress in the HP-DL also enhances the sinking of vacancies from the LP-TL. Note that this observation is in contrast to what was observed by Ott *et al.* [6] (who observed a uniform distribution of void sizes in the separation layer) and Labunov

et al. [2] (who observed the opposite trend of increasing void sizes in depth). The experimental conditions were however different.

Secondly, this void size enlargement at the top of the porous silicon layer is more prominent for the case of the thicker LP-TLs, which is obvious from the SEM images of Figure 7. 1 (a)-(c). This can be understood from the fact that in a thicker LP-TL, there are greater number of shrinking voids deeper in the LP-TL contributing to this void growth at the surface. Thus, an increase in the median void size at the surface is observed with increasing thickness of the LP-TL (Figure 7. 1 (d)). This trend continues to be true up to a LP-TL thickness of ~2 μm, at which point it appears to saturate. In the case of the thinnest LP-TL (i.e. 160 nm), the entire LP-TL interacts with the HP-DL and the surface, both of which act as vacancy sinks resulting in the shrinking of all LP-TL voids. Thus, no depth-dependent size distribution is observed for the thinnest LP-TL of the three shown in Figure 7. 1.

Thirdly, the LP-TL voids have only reached their equilibrium shape in the thinnest LP-TL sample (Figure 7. 1 (c)), characterized by clearly discernible faceting [11], [12]. In contrast, the majority of the voids in the thicker LP-TL samples are in constant flux (shrinking or growing), thus having random, non-equilibrium shapes.

Finally, while the voids in the thicker LP-TL samples are randomly stacked, the voids of the thinnest LP-TL are well-aligned in a single lateral array. These differences are expected to manifest in the quality of the LPL growth surface.

7.1.2.3 Surface topography of annealed porous silicon

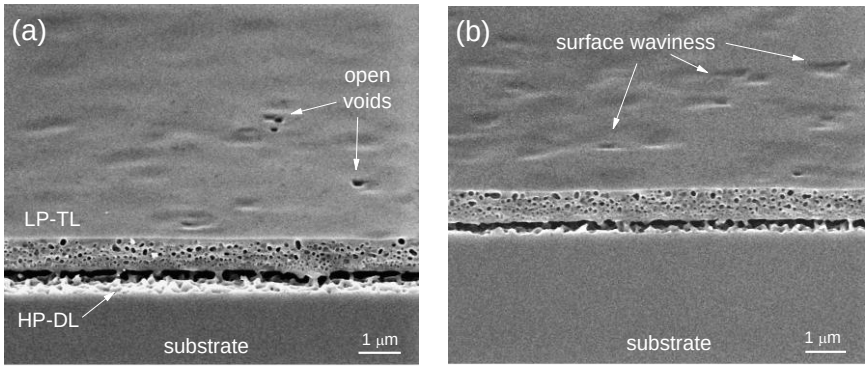

Figure 7. 2 Two tilted SEM images (a) and (b) taken at an angle of 20° from the plane of the porous silicon, showing the annealed porous silicon stack before epitaxial growth. The thickness of the LP-TL is ~750 nm. Open voids and surface waviness can be seen.

The surface topography of annealed porous silicon before epitaxial growth is imaged using SEM, as shown in Figure 7. 2. The surface of the LP-TL shows considerable amount of waviness. Moreover, defects such as open voids can be occasionally observed, where a LP-TL void remains open at the surface. This roughness and these defects will adversely impact the epitaxial growth process.

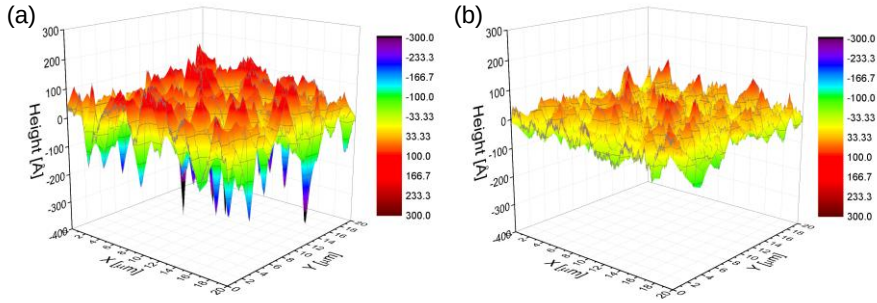

Figure 7. 3 Surface roughness maps measured using high resolution profilometry (using HRP-200 distributed by KLA Tencor) on the surface annealed porous silicon without epitaxial growth for a sample with a LP-TL of (a) 2100 nm and (b) 280 nm thickness.

The annealed LP-TL surface in four samples with different LP-TL thicknesses were analysed using high-resolution profilometry. The resulting surface roughness maps in a 2 µm by 2 µm area, in two of the samples with a LP-TL thickness of 2100 nm and 280 nm are shown in Figure 7. 3. The surface of the thinner LP-TL is observed to be much smoother than that of the thicker LP-TL.

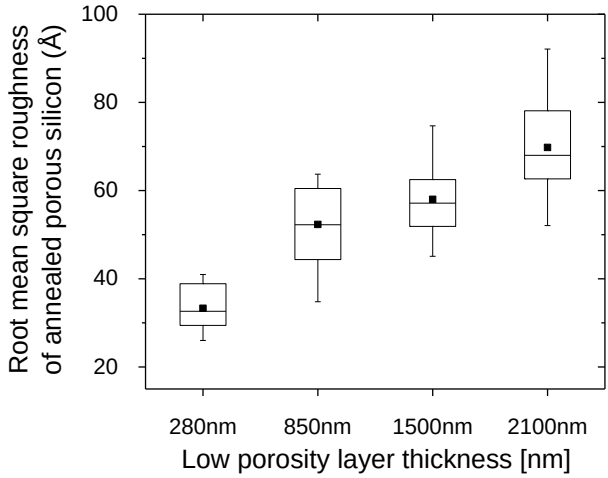

Figure 7. 4 The distribution of root-mean squared (RMS) values of the surface ordinates of the annealed LP-TL surface, calculated from more than 20 high resolution profilometry scans for four different LPL thicknesses, namely 280 nm, 850 nm, 1500 nm and 2100 nm. The three lines of the box plot refer to the 25th, 50th (median) and 75th percentiles and the lines/whiskers above and below the box extend to the 5th and 95th percentiles. The square symbol in the middle of the box plot refers to the mean value.

Figure 7. 4 shows the distribution of the RMS values for four different LP-TL thicknesses. Clearly, the surface roughness of the growth surface increases with the thickness of the LP-TL. This increase is attributed to the fact that the pores are larger and more misaligned in the thicker LP-TLs, as discussed previously. A similar trend in the peak-to-peak roughness values was also observed, with the

median peak-to-peak roughness increasing from ~18 nm for the thinnest LP-TL to ~35 nm for the thickest LP-TL investigated.

During epitaxy, the reactants are first adsorbed on the wafer surface where they react to form silicon atoms on the surface. This is followed by surface diffusion of the silicon atoms to the lowest energy sites on the surface, typically the edge of a step, leading to step flow growth. One of the factors determining the quality of the epitaxy is the surface diffusion rate relative to the arrival rate of the reactants. For high quality epitaxy, the surface diffusion rate should be much greater than the arrival rate of the reactants. In a rougher surface, the surface diffusion rate is reduced and this will lead to more defects in the epitaxial layer. Thus, it can be expected that thinner LP-TL templates should result in a better growth surface for epitaxy.

7.1.2.4 Residual stress in porous silicon

There have been reports on the presence of a residual tensile stress in electrochemically-etched porous silicon, shown experimentally using X-ray diffraction (XRD) [13] and micro-Raman spectroscopy [14] and explained theoretically by considering relaxation strain at the pore surfaces and thermal strain due to the difference in thermal expansion coefficients of silicon and porous silicon [9]. The residual stress is said to increase with pore size and has been reported to be in the range of a few hundred MPa up to 1-3 GPa [10], [14]. The ultimate tensile strength of silicon is ~7 GPa.

Porous silicon can be considered as a thin film on top of a silicon substrate. In thin films, intrinsic stress is usually in-plane and with the out-of-plane stress being negligible. Thus, the stress in porous silicon can be thought as a biaxial stress resulting in a biaxial in-plane strain.

Cross-sectional micro-Raman spectroscopy measurements were performed on epitaxial foils grown on two different LP-TL thicknesses: 850 nm and 1500 nm. In the absence of stress, the Raman peak for unstrained silicon occurs at a wavenumber of $\omega_0 = 520.75$ cm^{-1}. A shift in this wave number is a result of stress or change in crystallinity. Since the porous silicon layer is a quasi-monocrystal filled with voids, any peak shift is expected to be associated with a residual stress in porous silicon. The shift in the measured wavenumber ω relative to the unstrained silicon peak is then translated into stress values, σ according to [15]

$$\Delta\omega = \omega - \omega_0 = -2 \times 10^{-9}\sigma \tag{7.6}$$

The cross-sectional stress distribution maps of the epitaxial foil samples are shown in Figure 7. 5. Note that for the sample with a LP-TL thickness of ~850 nm, the entire porous silicon layer has been mapped (Figure 7. 5 (a)) while for the sample with a LPL thickness of ~1500 nm, only part of the LP-TL is shown in Figure 7. 5 (b). Several observations can be made from these maps. Firstly, a band of compressive stress (negative values) corresponding to the region around the HP-DL can be observed. Due to the relatively large spot size of ~1 μm compared to the 200 nm-thick HP-DL, it is not possible to conclude if this observed compressive stress is from the HP-DL or from the silicon surrounding this layer.

Secondly, the region above this band corresponds to the LP-TL, which is predominantly in tensile stress (positive values) with values in the range of 100-300 MPa. As mentioned above, this agrees well with investigations reported earlier. Note that in these measurements, the epitaxial foil was still well-attached to the substrate via the interconnections in the HP-DL. However, if these interconnections are broken and the epitaxial foil is detached at the HP-DL, the stress in the porous silicon is partially released. For example, when micro-Raman measurements were performed on the epitaxial foil of Figure 7. 5 (b) when the epitaxial foil has detached from the substrate, the tensile stresses measured in the LP-TL are only 50-100 MPa compared to 100-300 MPa observed before detachment.

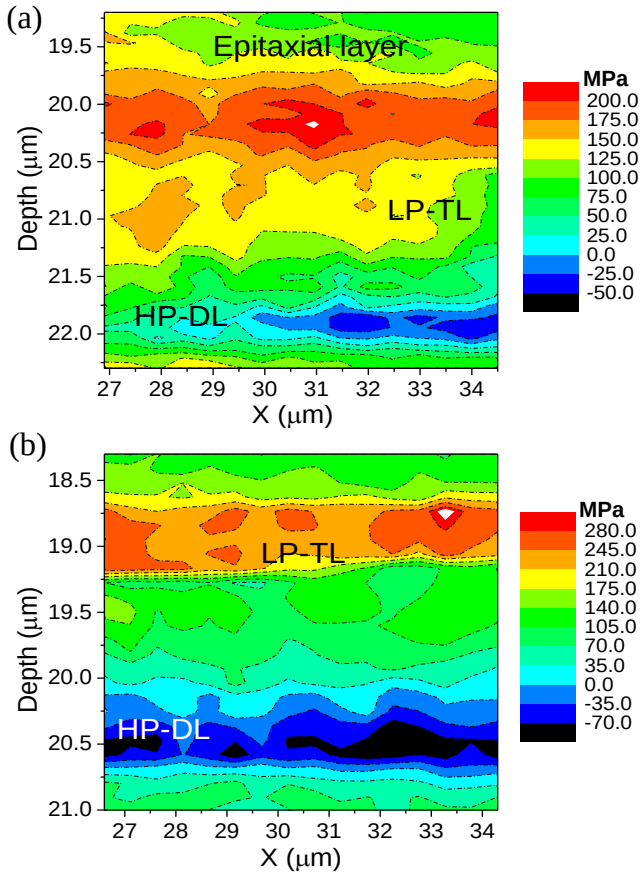

Figure 7. 5 Cross-sectional stress distribution maps obtained from micro-Raman spectroscopy measurements on epitaxial foil samples with a LP-TL thickness of (a) 850 nm and (b) 2100 nm.

X-ray diffraction measurements were also performed on the (001) wafer surface of two annealed LP-TLs with thicknesses of 850 nm and 1500 nm, to measure the out-of-plane stress. Figure 7. 6 shows the resulting intensity for the (004) Bragg reflection plotted against the scattering angle for the sample with a

LP-TL thickness of 1500 nm. An almost overlapping plot is obtained for the sample with a LP-TL thickness of 850 nm. Two distinct peaks are observed: the main peak corresponds to the silicon substrate while the smaller peak corresponds to porous silicon. Several low-intensity humps on either side of the silicon peak were also observed. Note that the tiny peaks visible in Figure 7. 6 are artefacts since the resolution used for the scan was too large to consider these as separate peaks.

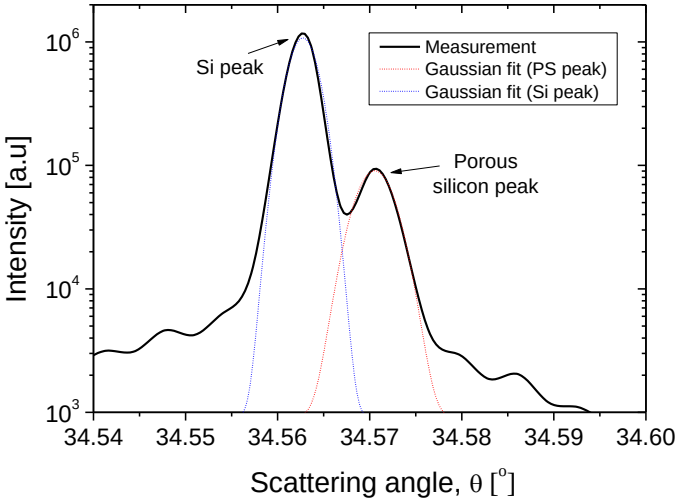

Figure 7. 6 Intensity of the (004) Bragg reflection plotted against the scattering angle from a high-resolution X-ray diffraction (HR-XRD) measurement with a $\theta - 2\theta$ scan in which the (001) wafer surface is irradiated with Cu K-alpha1 line with a wavelength of 1.54056Å. The two prominent peaks corresponding to the silicon substrate and the porous silicon are fitted with a Gaussian function.

The two prominent peaks in Figure 7. 6 have been fitted with Gaussian function. The scattering angle corresponding to the peak intensity of each of the two local maxima can be used to calculate the lattice parameter associated with silicon, d_{Si}, as well as porous silicon, d_{PS}, using the Bragg's law of diffraction

$$2d_i \sin\theta_B = n\lambda \tag{7.7}$$

where i stands for "Si" or "PS", $n = 4$ for the (004) Bragg reflection, θ_B is the scattering angle at peak intensity for each peak and λ is the wavelength of X-ray. For the Cu K-alpha1 emission line, λ =1.54056Å.

From the calculated lattice parameter values, the out-of-plane strain, ϵ_z, can be calculated as

$$\epsilon_z = \frac{d_{PS} - d_{Si}}{d_{Si}} \tag{7.8}$$

The strain calculated in this way, based on Figure 7. 6, is -1.978×10^{-4}, which implies a compressive out-of-plane strain. This agrees well with the micro-Raman measurements, where in-plane tensile stress was measured, which should lead to out-of-plane compressive strain. Based on the calculated strain value, an average in-plane biaxial stress, σ_r, can be computed (using cylindrical coordinates) with

$$\sigma_r = -\frac{B_{100}}{\nu}\epsilon_z \tag{7.9}$$

where B_{100} is the biaxial modulus corresponding to the crystal plane (100) given as 180 GPa [16] and ν is the Poisson's ratio, taken to be 0.28. This yields an in-plane biaxial tensile stress of ~127 MPa for the case of the LP-TL with a thickness of 1500 nm.

Comparing this with the stress distribution map from micro-Raman spectroscopy of Figure 7. 5 (b), there is correspondence between this value from XRD and the stress values in the uniform regions (green) of the LP-TL in the stress maps. A similar deduction can be made for the LP-TL with a thickness of 850 nm, with the average stress from XRD being ~120 MPa. However, micro-Raman measurements provide more insight into the stress distributions within the porous silicon, with local regions of much larger stress noticeable in the thicker LP-TL. In addition, it is noteworthy that the above procedure to obtain a single strain value from XRD measurements is not accurate since there will be a distribution of lattice parameters in the porous silicon stack.

Finally, a band of high tensile stress occurs in the region where the LP-TL transits into the epitaxial layer, as can be seen in Figure 7. 5 (a). This feature (not shown in Figure 7. 5 (b)) was observed in both samples. It should be noted that the measured stress distribution using micro-Raman spectroscopy itself gives an averaged value over a relatively large area of porous silicon (albeit with a better spatial resolution compared to XRD), the stresses in the porous silicon could actually be much higher locally and more widely distributed. Although the stress distribution is rather non-uniform, we can conclude that the epitaxial foil sample with a thicker LP-TL (Figure 7. 5 (b)) shows a higher average tensile stress compared to that with a thinner LP-TL (Figure 7. 5 (a)).

This has important implications for the quality of the epitaxial foil. Firstly, a higher stress in the porous silicon implies a larger strain (even if we assume negligible difference in the Young's modulus between the two LP-TLs) and hence a larger lattice mismatch between the porous silicon and the growing epitaxial silicon. Although the silicon epilayer will grow pseudomorphically at the beginning despite the slight lattice mismatch, the strain will eventually be relaxed via dislocations and stacking faults after the film has reached a critical thickness. Secondly, strain fields are intensified near sharp features [17]. Thus, a rougher porous silicon template (i.e. thicker LP-TL) with a similar intrinsic stress is likely to have local concentrations of higher stress at the growth surface. Thirdly, a thinner LP-TL with smaller pore size distribution (and possibly lower porosity (Figure 7. 1 (c))) is likely to be stiffer than a thicker LP-TL [18], [19]. A stiffer material with the same intrinsic stress will induce a lower amount of strain in the growing silicon epilayer. All of these support the fact that the intrinsic stress in porous silicon is likely to be more detrimental for epitaxial layers grown on thicker LP-TLs.

7.1.3 Reduction of the crystallographic defect density in epitaxial foils

In the previous sub-sections, it was shown that the thickness of the LP-TL layer can be varied to control the microstructure, surface topography as well as intrinsic stress in the porous silicon layer. To verify the impact of these properties of porous silicon on the quality of the epilayers, the crystallographic defect densities in epitaxial foils grown on different porous silicon templates were evaluated.

For this purpose, epitaxial layers grown on different LP-TLs were etched using the Wright solution [1], whose composition is such that the etch rate is much higher at crystallographic defects that meet the surface compared to defect-free locations. As a result, after 60-70 s of etching, topographic features form on the surface of the defect-etched epitaxial layers, revealing the presence of different types of defects. The main defects observed in the epifoils after defect etching are dislocations, stacking faults, multiple stacking faults and hillocks, which are shown in Figure 7. 7. Slip lines and orange peel defects were also observed among other defects. The square-shaped features and lines in Figure 7. 7 (a) correspond to etch pits where stacking faults meet the (100) silicon surface of the epifoil. The oval-shaped etch pits which appear as dots in the image are dislocations. Multiple stacking faults (shown in Figure 7. 7 (b)) are the superposition of numerous stacking faults around the same location, leading to a highly defected area. These are typical in locations where the LP-TL voids did not close completely. Hillocks form when a localised contaminant or defect on the growth surface accelerates the deposition rate of epitaxial silicon leading to the formation of a little mound of silicon.

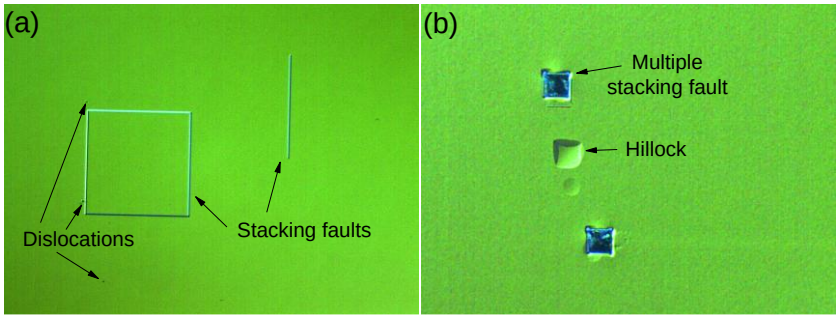

Figure 7. 7 Different interference contrast (DIC) optical microscopy images of the surface of defect-etched samples (using Wright solution) showing (a) stacking faults and dislocations in 20× magnification, and (b) multiple stacking faults and hillocks in 5× magnification. DIC mode enhances the visualisation of topographic features.

In a second defect etching run, three epitaxial foil samples with LP-TL thicknesses of 250 nm, 1500 nm and 2100 nm were analysed. By sampling more than 50 locations in a defect-etched area of 3 cm × 3 cm, the areal density of the various crystal defects were calculated and the results are shown in Figure 7. 8. There is a clearly observable reduction in all the crystal defects as the LP-TL thickness is reduced. The total defect density reduces from ~1230 defects/cm^2 in the sample with a 2100 nm-thick LP-TL to ~420 defects/cm^2 in the sample with a 250 nm-

thick LP-TL. This confirms the hypothesis that thinner LP-TLs result in smoother growth surfaces and lower intrinsic stress, allowing a higher quality epitaxial layer to be grown.

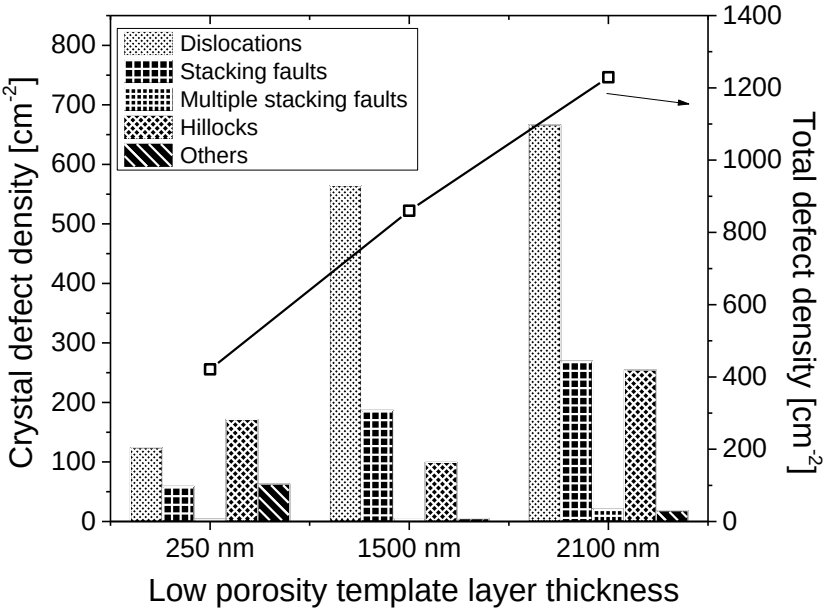

Figure 7. 8 Areal density of various crystal defects for epifoil samples grown on three different LP-TL thicknesses. The total defect density is depicted as line and should be read off on the vertical axis on the right side.

7.1.4 Enhancement of lifetime of epitaxial foils by tuning the porous silicon growth template

The ultimate figure of merit to benchmark the quality of the epifoil is minority carrier diffusion length or lifetime. Lifetime measurements were performed on two sets of glass-bonded, n-type, arsenic-doped (10^{16} cm^{-3}) epitaxial foils. The first set was obtained using the porous silicon-based layer transfer approach, while the second set was fabricated using lithography-based layer transfer process, which creates a pillar-free detachment layer, encapsulated by a void-free monocrystalline silicon seed layer, as explained in Chapter 6, Section 6.2.1 and shown in Figure 7. 9. Since the encapsulating layer is void-free, epifoils produced from this approach can act as a reference for the lifetime measurements on porous silicon-based epifoils. For the porous silicon-based epifoils, four different LP-TLs of the following thicknesses were used: 2100 nm, 1400 nm, 750 nm and 250 nm. Of these samples, only the three thickest samples detached, while the thinnest LP-TL of 250 nm thickness did not detach. Detachment issues will be addressed in Section 7.2.

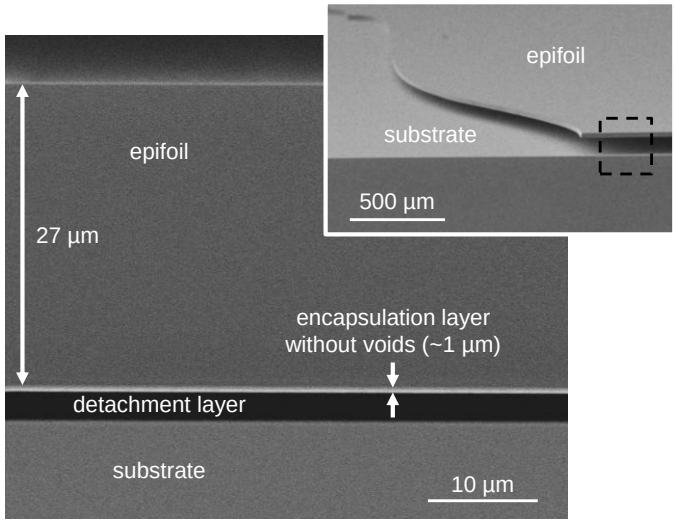

Figure 7. 9 Cross-sectional SEM image of the DUV lithography-based epifoil, showing pillar-free detachment layer and a void-free encapsulation layer. Inset: tilted view of the same sample at lower magnification.

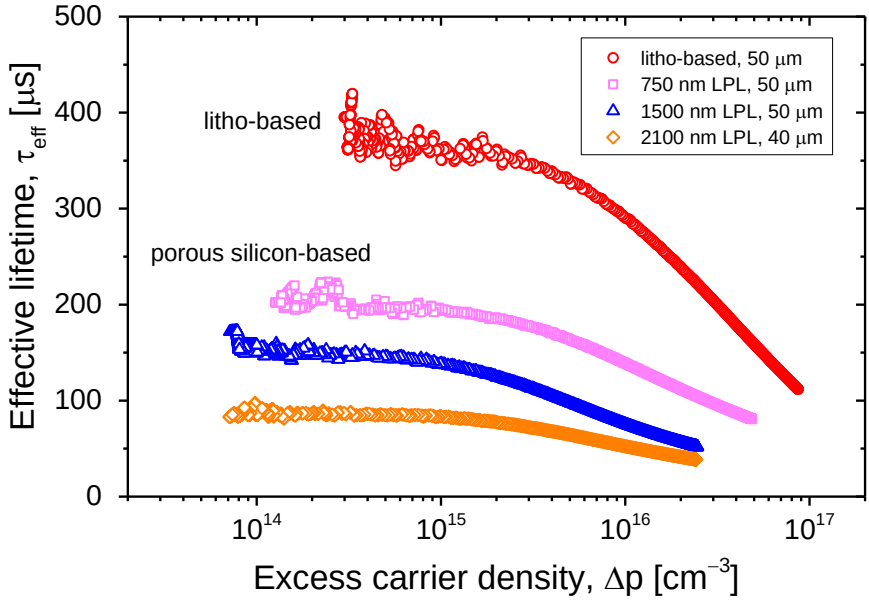

Figure 7. 10 Effective lifetimes as a function of injection level measured using QSSPC for porous silicon-based epifoils grown on three different porous silicon templates as well as lithography-based epifoils, confirming that higher quality epitaxial growth is obtained on thinner low-porosity template layers.

Lifetime measurements on both sets of epifoils were performed using quasi-steady state photoconductance (QSSPC) and the best lifetime results are plotted in

Figure 7. 10. Among the porous silicon-based epifoils, a clear trend in the effective lifetime is observed whereby the highest lifetime was measured in the epitaxial foil grown on the thinnest LP-TL that was still amenable for detachment (i.e. 750 nm-thick LP-TL) and reaches an excellent lifetime of ~195 μs at an injection level of 10^{15} cm^{-3}, whereas the epifoil with the thickest LP-TL of 2100 nm thickness only yielded ~85 μs at the same injection level. A comparison of the reference lithography-based epifoils with the porous silicon-based epifoils shows a drastic difference in the best lifetimes obtained thus far, with the lithography-based epifoils exceeding 350 μs at the injection level of 10^{15} cm^{-3}. Since both sets of epifoils are identical except for the template layer for epitaxial growth, we conclude that by reducing the LP-TL thickness, a drastic improvement in the lifetimes of porous silicon-based epifoils can be achieved.

7.2 Novel triple layer porous silicon stacks for easily-detachable, high lifetime epitaxial foils

7.2.1 Non-detachment of epitaxial foils on very thin porous silicon templates

As mentioned in Section 7.1.4, epitaxial foils grown on very thin (≤250 nm) LPL templates have detachment issues. Figure 7. 11 shows the detachment yield as a function of the low porosity template layer thickness. There is a trend towards increased detachment difficulty when the LP-TLs are made thinner.

The reason for this is that the LP-TL not only provides a crystal template for epitaxy, but also supplies vacancies for the increase in porosity of the HP-DL. For samples with a very thin LP-TL, the smaller volume of the LPL contributing to the enhancement of the porosity of the HPL results in a lower porosity in the HP-DL after annealing compared to a stack with thicker LP-TL. This results in a greater density of thicker interconnections or pillars in HP-DL bridging the LP-TL and the substrate, making detachment of epifoil samples on very thin LP-TLs difficult or impossible (Figure 7. 12 (a)). Conversely, the HP-DL of the thick LP-TL sample forms a pillar-free, elongated empty space under the LP-TL, allowing easy detachment (Figure 7. 12 (c)).

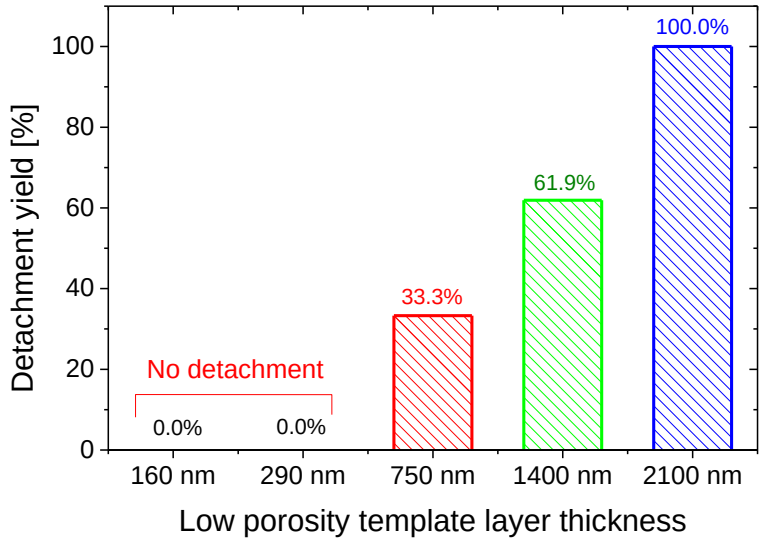

Figure 7. 11 Detachment yield for low porosity template layers of different thicknesses. Detachment yield decreases with decreasing low porosity layer thickness. The number of samples tested for each case (in order of increasing LP-TL thickness) is: 9, 3, 13, 21, and 23.

7.2.2 Strategies for achieving high lifetimes in detachable epitaxial foils

While thinner LP-TLs would result in higher lifetimes in epitaxial foils, this would lead to poor detachment yield, which is the most critical process step in LT-epicells. Thus, there seems to be a trade-off between ease of detachment and a better epitaxial growth template.

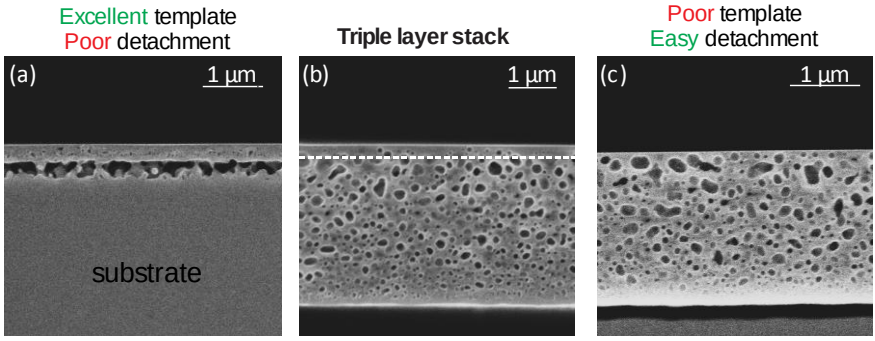

Figure 7. 12 SEM images of different porous silicon stacks. (a) and (c) are double layer stacks with an LP-TL thickness of 290 nm and 2100 nm respectively. The triple layer stack proposed in (b) combines the benefits of (a) and (c) by introducing a very low porosity third layer on top of an easily-detachable double-layer stack, allowing for both a good template for epitaxial growth and easy detachment.

This compromise is resolved by introducing a triple layer stack which combines the benefits of an easily detachable stack with a high quality epitaxial growth surface. In this novel stack, a thin, very low porosity layer is added on top of an

easily-detachable double layer stack such as the one with a LP-TL of 2100 nm thickness. After thermal reorganization, this top layer results in a dense silicon layer of ~100-180 nm thickness with very low density of tiny voids (< 50 nm), which makes for an excellent epitaxial growth template (Figure 7. 12 (b)). This third layer is now the template layer. The thick intermediate second layer now solely performs the role of a vacancy supply layer, resulting in the formation of a detachment plane with almost no pillars, allowing easy detachment.

In order to test the quality of these triple layers, defect density measurements were done. Two samples with a third layer of porous silicon on top of a typical double layer structure were prepared, one with a higher porosity and the other with a lower porosity. In this way, the direct correlation between the surface void size and lifetime can be made (rather than consider the entire porous silicon stack). The two different top layers were etched by using an applied current density of ~0.36 mA/cm^2 (denoted triple layer A) and ~6.9 mA/cm^2 (denoted triple layer B), respectively. The etching time for the two layers were 150s and 15s respectively.

The defect densities calculated for epitaxial layers grown on these triple layer templates are summarised in Figure 7. 13, where the results from Figure 7. 8 for samples with double layer templates are also included for comparison. For the triple layer sample A, it was observed that the overall defect density is significantly diminished to ~580 defects/cm^2 compared to a porous silicon template without this top lower porosity template layer (~860 defects/cm^2). In contrast, the sample with an additional 100 nm of higher porosity top layer (triple layer B), the defect density is significantly increased to ~3730 defects/cm^2.

By inspecting this porous silicon template of triple layer stack A (without an epilayer) using SEM (see Figure 7. 14), it was observed that the top 100 nm region was almost void-free and the original lower porosity top layer acted as a sacrificial layer to create a zone free of voids. This suggests that it is indeed the surface roughness and the stress distribution at the near surface region of the porous silicon that are critical in determining the crystal quality of the epitaxial foil. In typical double layer stacks, a 10 nm-thick void-free zone near the surface has been reported [6] but besides being much thinner than the triple layer approach, it is not uncommon to find sporadic defects such as open voids breaching this zone.

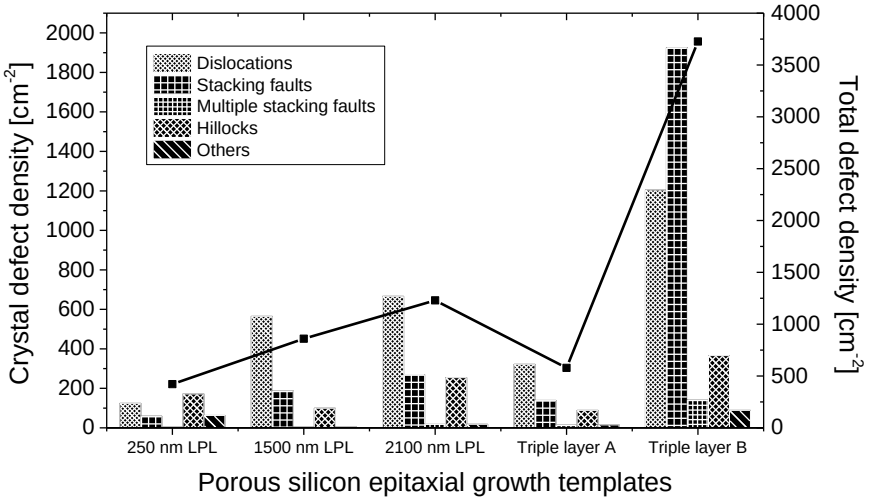

Figure 7. 13 Areal density of various crystal defects for epifoil samples with different porous silicon templates. The total defect density is depicted as line and should be read off on the vertical axis on the right side. Defect density results of double layered porous silicon stacks are repeated from Figure 7. 8 for comparison.

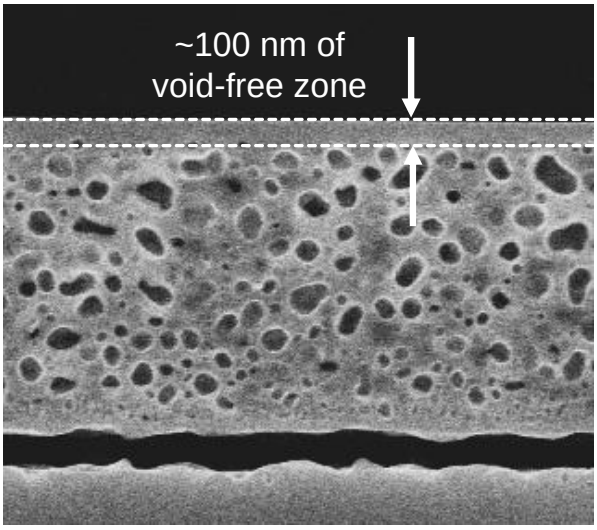

Figure 7. 14 Cross-sectional SEM image showing the porous silicon template for the trilayer layer A sample with a third layer of lower porosity than that of the LP-TL of a standard double layer porous silicon stack, showing ~100 nm of void-free zone near the surface.

Next, lifetime measurements were performed on such stacks, as shown in Figure 7. 15. As a reference, a double layer stack (without the third layer) is also been included. The results clearly show a correlation between epitaxial foil lifetime and surface void size and density, with the triple layer stack of Figure 7. 12 (b) showing higher lifetime compared to the other two. Note that the lifetime of the

reference sample itself is much higher than the previous experiments. This is because of continuous improvements made in passivation scheme as well epitaxial deposition conditions, as mentioned at the beginning of this chapter (see footnote in Section 7.1.1). However, samples are comparable within each experiment and when plotted together.

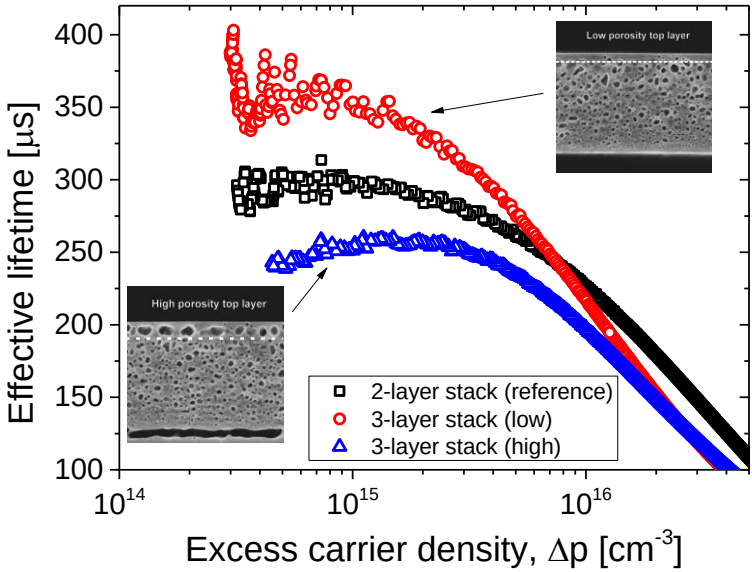

Figure 7. 15 Injection-level dependent lifetime measurements on epifoils grown on triple layer porous silicon stacks. A reference (double layer PS) is also included, since lifetimes are in general not comparable between two different experimental runs.

These effective lifetimes are among the highest reported in thin silicon epitaxial foils. It is also noteworthy that the triple layer stacks used for the lifetime measurements have a slightly thicker top layer, which has resulted in the sporadic breaching of the void-free zone by a small density of tiny voids. Thus, there appears to be an optimal thickness to achieve a void-free zone at the surface, depending of course on the porosity of this layer.

In conclusion, with this novel triple layer stack high quality epitaxial foils can be grown without compromising on the detachment yield, both of which are crucial for the success and viability of LT-epicells.

7.3 Chapter Summary

- The properties of porous silicon, particularly that of the low porosity template layer (LP-TL) significantly influences the quality of the epitaxial foil that is grown on top.

- Based on the classical sintering theory and vacancy diffusion processes, the reorganisation of porous silicon and the resulting morphology can be understood.
- A gradient of void sizes in depth is observed in the LP-TL, such that the largest voids are closest to the epitaxial growth surface.
- The thickness of the LP-TL is reduced systematically and the following observations were made:
    - Morphology: As the LP-TL thickness was reduced, the median surface void size also reduced. The voids were also more aligned and reached their equilibrium shapes for the thinnest LP-TL investigated.
    - Topography: The surface roughness also reduces with the LP-TL thickness. A smoother surface will allow a higher quality epitaxial growth.
    - Intrinsic stress distribution: The average stress in porous silicon, measured by micro-Raman spectroscopy, is lower in a thinner LP-TL. A growth surface that is less strained is better for epitaxy.
    - Defect density: As a result of the smoother surface and reduced stress in the porous silicon layer, the defect density in the epitaxial layer is also diminished. The best defect density measured on a ~250 nm thick LP-TL was ~420 defects/cm^2.
    - Minority carrier lifetime: The reduced defect densities in thinner LP-TL resulted in an consequent increase in the minority carrier lifetime. The highest effective lifetime measured on an n-type epitaxial foil at an injection level of 10^{15} cm^{-3} was 195 µs. This epitaxial layer was grown on a LP-TL with a thickness of 750 nm. However, this is still lower than that obtained for lithography-based epitaxial foils.
    - Very thin LP-TLs on which the best defect densities were measured could not be detached so that lifetime measurements can be performed. This is because reducing the LP-TL adversely affects the porosity of the high porosity detachment layer (HP-DL), since the LP-TL also functions as a vacancy supply layer.
- In order to achieve high lifetime epitaxial foils without compromising on detachment yield, a novel triple layer porous silicon stack is proposed.
    - In this concept, a third layer of porous silicon at the top with a very low porosity is introduced. The middle layer acts as the vacancy supply layer and is no longer a template layer.
    - With the new stack, 100% detachment yield has been achieved.
    - A good correlation of the effective lifetime with the surface porosity is attained.
    - The highest lifetimes obtained with the new stack is ~350 µs.
    - The triple layer stack was further optimised to produce a 100 nm thick void-free zone at the surface of the porous silicon stack, which should yield much higher lifetimes.

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Chapter 8
Conclusions and Perspectives

8.1 Porous silicon as a gettering layer

8.1.1 Main conclusions

Porous silicon gettering in the context of wafer-equivalent epitaxial silicon solar cells (WE-epicells) was studied both theoretically and experimentally. Improvement of the gettering efficiency is achieved by reducing the mean void size in the porous silicon layer. The following are the main conclusions from this work:

Theory and modelling of gettering (Chapter 2)

1. A procedure was presented to derive a metal contamination specification level for the maximum tolerable metal concentration in the low-cost substrate as well as in the feedstock used to crystallise the substrate, for a given target epitaxial layer minority carrier bulk lifetime. The analysis showed that implementing a metal gettering scheme is crucial in WE-epicells fabricated on low purity substrates, in order to mitigate epitaxial layer contamination.
2. Porous silicon gettering was described mathematically using equilibrium segregation thermodynamics.
3. The strength of metal gettering by porous silicon was studied using density functional theory (DFT). Large average binding energies for iron and copper of ~1.83 eV and ~2.07 eV were obtained, which corresponds to a large gettering efficiency, η_{gett}, of 7.5×10^2 for iron and 5.5×10^3 for copper.
4. Diffusion modeling based on the calculated binding energies and trap density confirmed the high gettering ratios expected.

Experimental proof of porous silicon gettering (Chapter 3)

5. Intentional contamination and gettering experiments were performed on epitaxial p/p^+ structures consisting of areas with and without embedded porous silicon on the same wafer. Iron, nickel and/or copper were used in the experimental work due to their ubiquity in low-cost substrates, high recombination activity, high solubility and high diffusivity in silicon.

6. Chemical / elemental analyses:
   a. Surface iron, nickel and copper concentration maps obtained using total reflection X-ray fluorescence (TXRF) of epitaxial p/p$^+$ samples contaminated (to high concentrations of $\sim 10^{16}$ cm^{-3}) from the backside through the substrate showed that very little or no metal impurities reached the top surface of the epitaxial layer in the areas with porous silicon. On the other hand, in areas without porous silicon, severe metal contamination, several orders of magnitude higher than the detection limit was observed, proving the efficacy of porous silicon gettering.
   b. Iron, nickel and copper concentration profiles in depth obtained using secondary ion mass spectroscopy (SIMS) on metal contaminated and gettered epitaxial p-type silicon/porous silicon/p$^+$ silicon substrate stack showed large accumulation of copper, iron and nickel in the porous silicon layer. Large gettering ratios of $>10^3$ for copper and nickel and $>10^2$ for iron were estimated, which corresponds very well with modeling predictions.
   c. A slower cooling rate was seen to result in better gettering characteristics.
7. Minority carrier lifetime measurements on iron and nickel contaminated samples:
   a. Iron gettering:
      i. For an [Fe] of $\sim 10^{13}$ cm^{-3}, the minority carrier lifetime of the epitaxial layer outside the porous silicon area dropped sharply after contamination, while that inside the porous silicon area remained stable. For an [Fe] of $\sim 10^{14}$ cm^{-3}, epitaxial layer lifetime in both areas reduced, but the effect was significantly lower in the porous silicon area.
      ii. Iron concentrations in the epitaxial layer were calculated based on the method of optical dissociation of iron-boron pairs together with lifetime measurements before and after dissociation. This reaffirmed a gettering efficiency of $> 10^2$ for iron, in agreement with SIMS analysis and modeling results, proving that the presence of porous silicon reduces the iron concentration in the epitaxial layer by orders of magnitude.
   b. Nickel gettering: Epitaxial layer bulk lifetimes were extracted by using a variation in the thickness of the epitaxial layers. For a [Ni] of $\sim 10^{13}$ cm^{-3}, the bulk lifetime of the epitaxial layer outside the porous silicon area dropped almost an order of magnitude after contamination, while that within the porous silicon area remained stable. However, for a [Ni] of $\sim 10^{14}$ cm^{-3}, the lifetimes in both areas were significantly affected, showing that porous silicon is only effective to a nickel concentration of up to $\sim 10^{13}$ cm^{-3}.

Enhancement of porous silicon gettering (Chapter 4)

8. DFT simulations on nano-voids of two different sizes showed that the most energetically-favourable binding sites exist in the edges and corners of a facetted void.
9. In the smaller void, there existed sites with binding energies much larger (e.g. 4.12 eV) than those obtained from simulation on the larger void. In these sites, greater dangling bond passivation is believed to increase the interaction energy of a metal atom to the surface trap site.

10. Experimentally, a sharp increase in the gettering efficiencies for copper, nickel with a reduction in void size is observed.
11. The increase in the binding energy is in inverse proportion to the void radius (i.e. a $1/r$-dependence). A binding energy enhancement of $\sim$288 meV for copper, $\sim$285 meV for nickel and $\sim$216 meV for iron were deduced when median void size is reduced from 39.8 to 27.2 nm. However, this could not be explained with simple curvature thermodynamics.
12. The $1/r$-dependence is due to the geometric scaling of the density of higher energy binding sites (which exist in corners and edges of facetted voids) which increase in inverse proportion to the void radius, agreeing well with the conclusions from DFT calculations.
13. Minority carrier lifetime measurements on samples gettered by porous silicon having different median void sizes were performed:
    a. Lifetime was higher in the sample gettered by porous silicon with a smaller mean void size. This was seen to hold for both iron and copper.
    b. For the iron-contaminated samples, the concentration of iron was found to be 3 times lower when the median void size of porous silicon is reduced from 40.0 to 36.7 nm.

Overall, it has been shown both theoretically and experimentally that porous silicon is a very efficient gettering layer for iron, nickel and copper, even at high temperatures. This is an important point because it means that gettering can occur simultaneously during epitaxy at 1130 ^{o}C and a dedicated high temperature gettering step is not needed. The gettering mechanism is a Langmuir-type surface chemisorption of metal atoms at void surface trap sites. Thus, the gettering is active at all metal concentrations and temperatures. The gettering efficiency can be enhanced significantly by reducing the average void size in the porous silicon layer, which can be done effortlessly. Finally, electrochemical etching of porous silicon is a comparatively inexpensive process. For these reasons, porous silicon as a gettering layer in WE-epicells is a crucial and viable option which helps to make WE-epicells an economically-attractive option.

8.1.2 Perspectives

In WE-epicells grown on low-cost substrates, porous silicon gettering is not the only technique that helps to reduce the metal contamination level in the epitaxial layer. Grain boundaries that exist in the substrate will also aid in metal gettering. In addition, if phosphorus diffusion is performed to create an emitter, this will also aid in the overall reduction of metal contamination in the epitaxial layer.

Since iron appears to be the most ubiquitous and detrimental impurity and it has a lower gettering efficiency than other metals, a strategy to significantly reduce the concentration of iron would be to perform porous silicon gettering multiple times. This would constitute a repetition of the following sequence multiple times: porous silicon forming – high temperature gettering – porous silicon removal. The number of times this is repeated is then a trade-off between the final cost and the final metal contamination level achieved.

Porous silicon gettering is not only important for WE-epicells but it can be applicable in general as an excellent gettering technique. For instance, in layer-transferred epitaxial silicon solar cells (LT-epicells), if the process flow is such that metallisation of the LT-epicell is performed before the detachment of the epitaxial layer from the parent substrate, then the parent substrate is under the risk of being metal contaminated. Here, porous silicon gettering could become useful before the substrate is re-used in the next layer transfer cycle.

8.2 Porous silicon as a template for epitaxy

8.2.1 Main conclusions

The potential for porous silicon as a template for high quality epitaxial growth of silicon, both in the context of wafer-equivalent epitaxial silicon solar cells (WE-epicells) and layer-transferred epitaxial silicon solar cells (LT-epicells) is studied and proven using minority carrier lifetime measurements. Improvement of the epitaxial layer quality by tuning the properties of porous silicon is shown. The following are the main conclusions:

Theory and modeling of lifetime measurements in epitaxial layers (Chapter 5)

1. The main constraints for lifetime measurements in epitaxial layers that are attached to the p^+ silicon substrate (as in WE-epicells) and those that are detached from the p^+ silicon substrate (as in LT-epicells) are identified and treated. For the case of "attached" epitaxial layers, the main constraint is the influence of the p^+ silicon substrate in the interpretation of the measurement results. For the case of "detached" epitaxial layers, the handling of thin silicon films and processing of complex structures involving silicone are the main challenges.
2. Attached epitaxial layers: minority carrier lifetime using two measurement methods, namely, simulation-assisted steady-state photoluminescence (sim-PL) and microwave-detected photoconductance decay (μ-PCD) on p/p^+ structures are considered. Porous silicon is expected to influence both the bulk quality of the epitaxial layer and the level of interface recombination at the p/p^+ silicon interface. Thus, efforts are made to decouple the bulk lifetime, τ_{epi}, and the sum of effective surface and effective interface recombination velocities, S_{tot}, to discriminate the effect of porous silicon on each component. As reference, epitaxial layers grown on pristine silicon (without porous silicon) are used for comparison.
    a. Simulation-assisted steady-state photoluminescence: this steady-state method was first proposed by Rosenits *et al.* [1] for evaluating bulk lifetime of p-type epitaxial layers on pristine p^+ silicon. It is based on measuring the ratio of PL intensities from epitaxial p/p^+ silicon samples with two different epitaxial layer thicknesses and relating it to bulk lifetimes with the aid of numerical simulations. This work is developed in greater depth in the work of this thesis for p-type epitaxial layers grown on pristine p^+ silicon as well as porous silicon.

i. The procedure to decouple τ_{epi} and S_{tot} from the PL intensity measurements is described for the case of a p-type epitaxial layer grown on pristine silicon (low interface recombination) and for one that is grown on annealed porous silicon (high interface recombination).

ii. A theoretical framework to describe the emission of PL in an epitaxial p/p^+ structure is discussed.

iii. The contribution of the PL signal emitted by the substrate is shown to influence the measured signal significantly in cases when there is no porous silicon. Based on the theoretical framework, an elegant method for subtracting the substrate PL signal from the total measured signal is proposed.

b. Microwave-detected photoconductance decay (μ-PCD): in this transient method, the effective lifetime of the epitaxial layer is measured. Measurements on epitaxial layers of different thicknesses are used to decouple the bulk lifetime and the sum of effective surface and effective interface recombination velocities.

i. It is shown that the substrate does not influence the measurements due to the high doping densities and the measured effective lifetime represents that of the epitaxial layer.

ii. The issues with decoupling $\tau_{epi}$and S_{tot} using this method are described.

c. Detached epitaxial layers: minority carrier lifetime measurements are performed using quasi-steady state photoconductance (QSSPC) and calibrated PL. A methodology for measurement of thin epitaxial foils in a glass-bonded configuration is described. A method to decouple $\tau_{epi}$and S_{tot} is also described. However, since the porous silicon layer is removed before passivation and measurements, effective lifetime itself should be a good measure of the bulk quality of the detached epitaxial layers. As reference, a lithography-based epitaxial foil whose seed layer is void-free and whose detachment plane is pillar-free is used for comparison.

Experimental proof of high minority carrier lifetimes in epitaxial layers grown on annealed porous silicon (Chapter 6)

3. Attached epitaxial layers:

a. It is shown that the bulk lifetime of an epitaxial layer grown on an annealed porous silicon Bragg reflector stack is comparable to that grown on pristine silicon. For epitaxial layers grown on mirror-polished monocrystalline Czochralski silicon, the bulk lifetimes of p-type of epitaxial layers are in the range of ~100-125 μs (i.e. 535-600 μm diffusion length which is 10-15 times the epitaxial layer thickness). This shows that the porous silicon Bragg reflector stack is not only optimised for reflection but also for high quality epitaxial growth.

b. However, the interface recombination at a p/p^+ interface with an annealed porous silicon embedded inside the p^+ layer is extremely high with an effective interface recombination velocity of ~10^4-10^5 cm/s, which is

similar in value to an unpassivated surface. This shows that porous silicon detrimentally enhances the interface recombination of minority carriers.

c. With the inclusion of an epitaxially-grown back surface field with a doping concentration of 10^{19} cm^{-3} and a thickness of ~2 µm on top of the annealed porous silicon, the effective interface recombination velocity improves to < 10^3 cm/s, more than an order of magnitude to an unshielded interface.

d. A model to describe the effective interface recombination velocity of a BSF-protected p/p$^+$ interface with an embedded porous silicon is derived and verified.

e. Both lifetime measurements methods have their limitations. The technique of sim-PL only allows ballpark values for S_{tot} to be evaluated and is insensitive to S_{tot} when $S_{tot} < 10^3$ cm/s. The technique of µ-PCD, on the other hand, is insensitive to τ_{epi} when $S_{tot} > 10^3$ cm/s, but precise values for S_{tot} can be obtained.

4. Detached epitaxial layers:

a. Processing glass-bonded epitaxial foils in such a way that silicone is well-shielded is shown to be important for obtaining high quality surface passivation which is crucial for reliable lifetime measurement results.

b. The effective lifetime of n-type epitaxial layers grown on standard annealed porous silicon stacks used in the layer transfer process result in values up to ~140 µs (~400 µm diffusion length) at the injection level of 10^{15} cm^{-3}. However, this is much lower than the values obtained for reference lithography-based epitaxial foils which attain up to ~350 µs (i.e. ~630 µm diffusion length) at the same injection level. This shows that the porous silicon layer for this cell concept is optimised for layer transfer and is not optimal for high quality epitaxial growth.

Enhancement of the bulk quality of epitaxial foils grown on annealed porous silicon (Chapter 7)

5. The porous silicon properties, in particular the thickness and porosity, were tuned in order to produce a better growth template at the surface of the annealed porous silicon, where epitaxial growth takes place.

6. Morphology and topography: a reduction in the thickness of the low porosity template layer (LP-TL) resulted in a reduction in the median surface void size near the epitaxial growth surface and the root-mean-square surface roughness of the porous silicon template.

7. Stress in porous silicon: the reduction in the LP-TL thickness also resulted in a corresponding reduction in the average stress in the porous silicon layer, measured using micro-Raman spectroscopy and X-ray diffraction.

8. Defect density: a smoother growth surface and a porous silicon layer with lower strain resulted in better quality epitaxial growth. Defect-etched epitaxial layers grown on porous silicon templates with different LP-TL thicknesses showed a reduction in the overall defect density with reduction in LP-TL thickness. The best defect density of ~420 defects/cm^2 was observed in an epitaxial layer grown on a LP-TL with a thickness of ~250 nm.

9. Minority carrier lifetime: an improvement in the minority carrier lifetime of n-type epitaxial foils corresponding to a reduction in LP-TL thickness was achieved. The best effective lifetime of ~195 µs (i.e. 470 µm diffusion length) at an injection level of 10^{15} cm^{-3} was achieved on an 50 µm thick n-type epitaxial foil grown on a porous silicon template with a 750 nm thick LP-TL.
10. Non-detachment of thin porous silicon templates: a reduction in the LP-TL results in the reduction of the porosity of the high porosity detachment layer (HP-DL) which makes detachment of very thin templates (e.g. a porous silicon template with a 250 nm thick LP-TL) impossible.
11. A novel triple layer porous silicon stack: a three-layer stack is proposed in place of the standard double layer stack. The newly-introduced top layer functions as the template layer. The middle layer acts as the vacancy supply layer during thermal reorganisation to increase the porosity of the detachment layer. The third layer has a much lower porosity and is tuned such that a void-free zone of ~100 nm is formed at the top surface, which makes for a better epitaxial growth template, while allowing easy detachment of the epitaxial layer. The highest lifetime obtained with such a stack is ~350 µs (~670 µm diffusion length) at an injection level of 10^{15} cm^{-3} on a 40 µm thick n-type epitaxial foil.

In summary, it has been shown high quality epitaxial layers can be grown on annealed porous silicon both in the case of WE-epicells as well as LT-epicells. For attached epitaxial layers, the bulk quality of the epitaxial layer is not adversely affected by the embedded porous silicon. However, the interface recombination is exacerbated by its presence, even if a back surface field shields the minority carriers from the interface. This disadvantage is overcome in the LT-epicells where detachment at the porous silicon layer allows access to the interface so that the porous silicon can be removed and the epitaxial layer well passivated on both surfaces. However, the porous silicon stack used in a standard LT-epicell is not well-optimised and the properties of the porous silicon influence the bulk quality of the epitaxial foil significantly. The novel triple layer porous silicon stack proposed in this thesis is not only a better template for epitaxial growth but also allows easier detachment of epitaxial foils, resulting in a higher detachment yield for the layer transfer process. The only change that this triple layer stack introduces in the process flow of LT-epicells is a longer etch time for the electrochemical etching of porous silicon.

8.2.2 Perspectives

Further tuning of the porous silicon morphology towards that of the lithography-based template can result in a further improvement of the minority carrier lifetime and diffusion length in the epitaxial foils. This work is ongoing but could not be finished in the time frame of this thesis.

These studies were done on high quality mirror-polished wafers. The validity of the improvements must be tested on chemically-polished wafers. This is because parent substrates are to be re-used multiple times for layer transfer of epitaxial layers and after the first use, the surface of the parent substrate is conditioned by

chemical polishing for subsequent re-uses. Further optimisation of the porous silicon template there-on must be performed to achieve similar improvements.

The implication of the minority carrier lifetime and diffusion length improvements at the level of the cell efficiency needs to be proven. However, at the moment, a stable baseline process does not exist for this to be tested.

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List of 1st author publications

(as of 4 March 2014)

Peer-reviewed publications

[1] H. Sivaramakrishnan Radhakrishnan, C. Ahn, J. Van Hoeymissen, F. Dross, N. Cowern, K. Van Nieuwenhuysen, I. Gordon, R. Mertens, and J. Poortmans, "Gettering of transition metals by porous silicon in epitaxial silicon solar cells," *Physica Status Solidi*, vol. 209, no. 10, pp. 1866–1871 (2012).

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Award

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